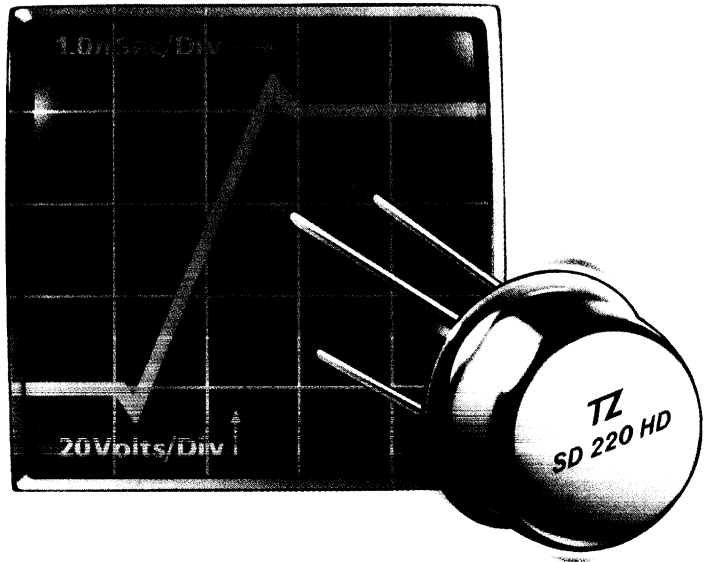


DMOS



1988 DATA BOOK

TOPAZ
SEMICONDUCTOR

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SECTION 1

TOPAZ SEMICONDUCTOR

Topaz Semiconductor Inc. was founded in March of 1985. The company specializes in design and manufacturing high performance devices for high frequency analog signal processing and medium power, high voltage transistors and smart power circuits. The technologies used are double-diffused MOS, (D-MOS) and D-MOS integrated with complementary MOS, (CMOS/D-MOS).

The D-MOS process can be utilized to reduce gate length (lateral D-MOS) or to increase transistor breakdown voltage (vertical D-MOS). Short gate length increases the speed of lateral D-MOS devices beyond that achievable with other silicon structures. Hence, lateral D-MOS FETs can provide a performance bridge between other silicon devices and GaAs devices. Lateral D-MOS devices are used extensively in applications ranging from large signal analog switching, (RF, video, ATE, telephone, etc.), to small signal VHF/VHF amplifiers, and high-speed digital interface applications, such as pin drivers in automatic test equipment and logic analyzer probes.

Depletion mode, (normally-ON), lateral D-MOS FETs can be substituted for J-FETs in many applications and extend high frequency performance by an order of magnitude.

Vertical D-MOS can operate at high voltages, over 600V, yet can be controlled by small amplitude, very low current signals. Topaz Semiconductor specializes in ultra low leakage, low threshold and multiple chip configurations used in back plane testers, signal analyzers, solid state relays and display driver applications.

Vertical D-MOS devices with gate-source standoff voltage above 100 volts are used as replacements for reed relays. Another application is high voltage switching without level shifting.

CMOS/D-MOS integrated circuits feature high off isolation at video frequencies combined with low insertion loss. The major applications are in video and RF switching. On chip control of high frequency signal switching reduces crosstalk between channels and increases the level of integration.

Topaz Semiconductor has a state-of-the-art, class 10, 5" wafer fabrication line located at its San Jose facility. The company's focus is on development of new, higher performance products within selected market segments, i.e., signal processing and smart power areas. The key element in this strategy is the utilization and further enhancement of D-MOS technology.

Topaz Semiconductor manufactures a large number of standard D-MOS and CMOS/D-MOS products. Some of the new products are designed to be compatible with existing industry standard devices. When used in place of those standard parts, they provide an economical way of extending performance of existing systems.

In addition to standard catalog parts, Topaz Semiconductor also manufactures application specific products, offers special processing and selections, and high reliability products tested to military requirements.

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SD1113CHP	CHIP	D-MOS FET N-CHAN 200V 10 ohm	3-73
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SD1115DD		DISCONTINUED, REPLACED BY SD1107DD	
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SD212DE	TO-72	D-MOS FET N-CHAN 10V 70 ohm	3-50
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SD5200CHP	CHIP	QUAD D-MOS FET N-CHAN 30V 80 ohm Z	3-116
SD5200N	16-PDIP	QUAD D-MOS FET N-CHAN 30V 80 ohm Z	3-116

TOPAZ PART TYPE	PACKAGE	DESCRIPTION	DATA SHEET PAGE NO.
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SD5401CY	SO-14	QUAD FET N-CHAN 10V 30 ohm COMM TEMP	3-118
SD5402CY	SO-14	QUAD FET N-CHAN 15V 30 ohm COMM TEMP	3-118
SD5501CHP	CHIP	QUAD D-MOS N-CHAN DEPL 20V, 150 ohm	3-121
SD5501J	16-CDIP	QUAD D-MOS N-CHAN DEPL 20V, 150 ohm	3-121
SD5501N	16-PDIP	QUAD D-MOS N-CHAN DEPL 20V, 150 ohm	3-121
SST211	SOT-143	D-MOS FET N-CHAN 30V 70 ohm ZENER	3-123
SST213	SOT-143	D-MOS FET N-CHAN 10V 70 ohm ZENER	3-123
SST215	SOT-143	D-MOS FET N-CHAN 20V 70 ohm ZENER	3-123
TN0106N3	TO-92	D-MOS FET N-CHAN 60V 3.0 ohm	3-86
TN0106ND	CHIP	D-MOS FET N-CHAN 60V 3.0 ohm	3-86
TN0110N3	TO-92	D-MOS FET N-CHAN 100V 3.0 ohm	3-86
TN0110ND	CHIP	D-MOS FET N-CHAN 100V 3.0 ohm	3-86
TZ400BD	TO-92	D-MOS FET N-CHAN 30V, 80 ohm ZENER	3-125
TZ402BD	TO-92	D-MOS FET N-CHAN 15V, 80 ohm ZENER	3-125
TZ403BD	TO-92	D-MOS FET N-CHAN 15V, 60 ohm ZENER	3-128
TZ404BD	TO-92	D-MOS FET N-CHAN 20V 8.0 ohm ZENER	3-131
TZ404CY	SOT-89	D-MOS FET N-CHAN 20V 8.0 ohm ZENER	3-131
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VN0106N3	TO-92	D-MOS FET N-CHAN 60V 3.0 ohm	3-138
VN0106ND	CHIP	D-MOS FET N-CHAN 60V 3.0 ohm	3-138
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VN10LM	TO-237	D-MOS FET N-CHAN 60V 5.0 ohm	3-144
VN2222LL	TO-92	D-MOS FET N-CHAN 60V 7.5 ohm	3-140
VN2222LM	TO-237	D-MOS FET N-CHAN 60V 7.5 ohm	3-144
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VN2410M	TO-92	D-MOS FET N-CHAN 240V, 10 ohm	3-146
VP0104N3	TO-92	D-MOS FET P-CHAN -40V, 8.0 ohm	3-149
VP0104ND	CHIP	D-MOS FET P-CHAN -40V, 8.0 ohm	3-149
VP0106N3	TO-92	D-MOS FET P-CHAN -60V, 8.0 ohm	3-149
VP0106ND	CHIP	D-MOS FET P-CHAN -60V, 8.0 ohm	3-149
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VP0109ND	CHIP	D-MOS FET P-CHAN -90V, 8.0 ohm	3-149
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VP0540ND	CHIP	D-MOS FET P-CHAN -400V, 75 ohm	3-152
VP0808CHP	CHIP	D-MOS FET P-CHAN -80V, 5.0 ohm	3-156

TOPAZ PART TYPE	PACKAGE	DESCRIPTION	DATA SHEET PAGE NO.
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VP0808M	TO-237	D-MOS FET P-CHAN -80V, 5.0 ohm	3-156
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VP1008L	TO-92	D-MOS FET P-CHAN -100V, 5.0 ohm	3-156
VP1008M	TO-237	D-MOS P-CHAN -100V 5.0 ohm	3-156
VQ1000J	14-PDIP	QUAD D-MOS FET N-CHAN 60V, 5.5 ohm	3-159

SECTION 2

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PRODUCT SELECTOR GUIDE	2-2
PRODUCT SUBSTITUTION GUIDE	2-3
PRODUCT DATA SHEETS	2-4 to 2-47

ANALOG SWITCHES

Type No..	Temp. Range	Package	Config.	Logic '0'	Logic Levels (Volts)	r _{DS(ON)} Typ. (ohms)	Off(1) Isolation (dB)	Analog Range (Volts)	Switch Bandwidth (MHz)
CDG201AK	MIL	16-CDIP	4xSPST	ON	0.8-2.4	45	66	+10,-10	100
CDG201BJ	IND	16-PDIP	4xSPST	ON	0.8-2.4	45	66	+10,-10	100
CDG201BK	IND	16-CDIP	4xSPST	ON	0.8-2.4	45	66	+10,-10	100
CDG201CJ	COMM	16-PDIP	4xSPST	ON	0.8-2.4	45	66	+10,-10	100
CDG211CJ	COMM	16-PDIP	4xSPST	ON	0.8-2.4	45	66	+10,-10	100
CDG211DY	E. IND.	S0-16(3)	4xSPST	ON	0.8-2.4	45	66	+10,-10	100
CDG308AK	MIL	16-CDIP	4xSPST	OFF	1.0-4.5	45	62	+10,-10	100
CDG308BJ	IND	16-PDIP	4xSPST	OFF	1.0-4.5	45	62	+10,-10	100
CDG308CK	IND	16-CDIP	4xSPST	OFF	1.0-4.5	45	62	+10,-10	100
CDG308CJ	COMM	16-PDIP	4xSPST	OFF	1.0-4.5	45	62	+10,-10	100
CDG308DY	E. IND.	S0-16(3)	4xSPST	OFF	1.0-4.5	45	62	+10,-10	100
CDG309AK	MIL	16-CDIP	4xSPST	ON	1.0-4.5	45	62	+10,-10	100
CDG309BJ	IND	16-CDIP	4xSPST	ON	1.0-4.5	45	62	+10,-10	100
CDG309BK	IND	16-CDIP	4xSPST	ON	1.0-4.5	45	62	+10,-10	100
CDG309CJ	COMM	16-CDIP	4xSPST	ON	1.0-4.5	45	62	+10,-10	100
CDG309DY	E. IND.	S0-16(3)	4xSPST	ON	1.0-4.5	45	62	+10,-10	100
CDG2214AK	MIL	8-CDIP	1xSPST	ON	1.0-4.5	45	82	+10,-10	250
CDG2214BJ	IND	8-PDIP	1xSPST	ON	1.0-4.5	45	82	+10,-10	250
CDG2269CJ(2)	COMM	16-PDIP	2xSPDT		1.0-4.5	20/40	42	+10,-10	200
CDG2269CY(2)	COMM	S0-16(3)	2xSPDT		1.0-4.5	20/40	42	+10,-10	200
CDG4308BJ	IND	20-PDIP	4xSPST	OFF	1.0-4.5	45	68	+10,-10	100
CDG4309BJ	IND	20-PDIP	4xSPST	ON	1.0-4.5	45	68	+10,-10	100
CDG5341AK	MIL	14-CDIP	Dual T	OFF	1.0-4.5	110	80	+10,-10	50
CDG5341BJ	IND	14-PDIP	Dual T	OFF	1.0-4.5	110	80	+10,-10	50
CDG5341BK	IND	14-CDIP	Dual T	OFF	1.0-4.5	110	80	+10,-10	50
CDG5341CJ	COMM	14-PDIP	Dual T	OFF	1.0-4.5	110	80	+10,-10	50

Note 1: RL = 50 ohms, f = 10MHz Note 2: Includes Data Latch Note 3: Surface Mount Package

ANALOG MULTIPLEXERS

Type No.	Temp. Range	Package	Config.	Logic Levels (Volts)	r _{DS(ON)} Typ. (ohms)	Cross(1)(2) Talk (dB)	Analog Range (Volts)	Switch Bandwidth (MHz)
CDG4500AK	MIL	14-CDIP	4-Channel	1.0-4.5	40	62	+10,-10	100
CDG4500BJ	IND	14-PDIP	4-Channel	1.0-4.5	40	62	+10,-10	100
CDG4500BK	IND	14-CDIP	4-Channel	1.0-4.5	40	62	+10,-10	100
CDG4500CJ	COMM	14-PDIP	4-Channel	1.0-4.5	40	62	+10,-10	100

Note 1: R_L = 50 ohms, f = 10MHz

Note 2: All Channels, Single Channel 80dB

DIGITAL CONTROLLED ATTENUATORS

Type No.	Package	Logic Levels (V)	Parallel Data Bits	Attenuation		MAX. Analog Input (V)	MAX. Frequency (MHz)
				Per Step (dB)	Range (dB)		
CDG4460J	Special, 16-Pin Ceramic	1.0-4.5	6	0.25	0-15.75	+4.0,-4.0	40-60
CDG4469J	Special, 16-Pin Ceramic	1.0-4.5	8	0.50	0-127.5	+9.0,-9.0	0.2-0.5

TYPE NO.	SOURCE	CONFIGURATION	PACKAGE	TOPAZ TYPE NO.
ADG201ABQ	1	4 x SPST	16-CDIP	CDG201BK
ADG201AKN	1	4 x SPST	16-PDIP	CDG201CJ
ADG201ATQ	1	4 x SPST	16-CDIP	CDG201AK
DG201A Series	6	4 x SPST		CDG201 Series
DG201AAK	10	4 x SPST	16-CDIP	CDG201AK
DG201ABK	10	4 x SPST	16-CDIP	CDG201BK
DG201ACJ	10	4 x SPST	16-PDIP	CDG201CJ
DG201ACK	10	4 x SPST	16-CDIP	CDG201BK
DG211	6	4 x SPST		CDG211CJ
DG211CJ	10	4 x SPST	16-PDIP	CDG211CJ
DG271BK	10	4 x SPST	16-CDIP	CDG201BK
DG271CJ	10	4 x SPST	16-PDIP	CDG201CJ
DG271CK	10	4 x SPST	16-CDIP	CDG201BK
DG308AAK	10	4 x SPST	16-CDIP	CDG308AK
DG308ABK	10	4 x SPST	16-CDIP	CDG308BK
DG308ACJ	10	4 x SPST	16-PDIP	CDG308CJ
DG308ACK	10	4 x SPST	16-CDIP	CDG308BK
DG309AK	10	4 x SPST	16-CDIP	CDG309AK
DG309BK	10	4 x SPST	16-CDIP	CDG309BK
DG309CJ	10	4 x SPST	16-PDIP	CDG309CJ
DG309CK	10	4 x SPST	16-CDIP	CDG309BK
DGP201AAK	10	4 x SPST	16-CDIP	CONTACT FACTORY
DGP201ABK	10	4 x SPST	16-CDIP	CONTACT FACTORY
DGP201ACJ	10	4 x SPST	16-PDIP	CONTACT FACTORY
HT201-2 Series	4	4 x SPST		CDG201 Series
HI201-5 Series	4	4 x SPST		CDG201 Series
HI201-2 Series	4	4 x SPST		CDG201 Series
HI201HS-5 Series	4	4 x SPST		CDG201 Series
IH5341 Series	6	2 x SPST DUAL T		CDG5341 Series
IH5341CPD	4	2 x SPST DUAL T	14-PDIP	CDG5341CJ
LF11201D	8	4 x SPST	16-CSB	CDG201AK
LF13201D	8	4 x SPST	16-CSB	CDG201BK
LF13201N	8	4 x SPST	16-PDIP	CDG201CJ
MP201DIAP	7	4 x SPST	16-CDIP	CDG201AK
MP201DIBP	7	4 x SPST	16-CDIP	CDG201BK
MP201DICJ	7	4 x SPST	16-PDIP	CDG201CJ
SW-201F Series	9	4 x SPST		CDG201 Series
SW-201G Series	9	4 x SPST		CDG201 Series

SOURCE

1—Analog Devices
3—Harris Semiconductor
4—GE/Intersil
6—Maxim

7—Micropower
8—National Semiconductor
9—Precision Monolithics
10—Siliconix

QUAD MONOLITHIC SPST CMOS/D-MOS ANALOG SWITCH

ORDERING INFORMATION

Package	CDG201	CDG201AK
Pin Range	1-16	1-16
Temp. Range	-40 to 125	-40 to 125

FEATURES

- High OFF Isolation, 66 dB @ 10MHz
- Wide Bandwidth Switches, 0.9 x DC @ 100MHz
- Low Channel-to-Channel Crosstalk, -80 dB @ 10MHz
- TTL Compatible
- Industry Standard Pin-Out

APPLICATIONS

- Glitch-Free Analog Switches
- RF & Video Switches
- Track and Hold Switches
- Sample and Hold Switches

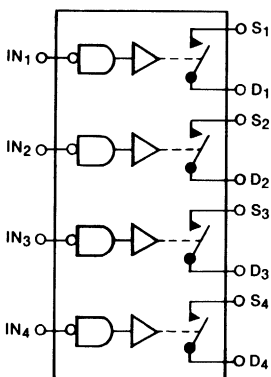
DESCRIPTION

The Topaz Semiconductor CDG201 Analog Switch features TTL compatible input logic and wide-band Lateral D-MOS switches on a single chip. The on-chip reference used for TTL compatibility gives the added advantage of constant logic switching over a wide range of supply voltages and temperature without a separate power supply. Industry standard pin-out makes the CDG201 particularly suitable for replacement of existing analog switches and at the same time upgrading high frequency performance.

NOTE

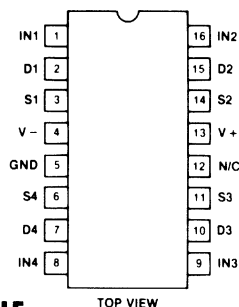
All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic level (V_{DD} or GND).

FUNCTIONAL BLOCK DIAGRAM



Four SPST Switches per Package
Switches shown in Logic "1" Input Position

PIN CONFIGURATION



LOGIC TABLE

Logic	Switch	
0	ON	Logic '0' \cong 0.8V
1	OFF	Logic '1' \cong 2.4V

ABSOLUTE MAXIMUM RATINGS

V⁻ Negative Supply Voltage -20V
 V⁺ Positive Supply Voltage +20V
 V_{IN} Control Input Voltage Range V⁺ +0.3V,
 V⁻ -0.3V
 I_L Continuous Current, any Pin
 Except S or D 20 mA
 I_S Continuous Current, S or D 30 mA
 I_S Peak Pulsed Current, S or D,
 80μsec, 1%, Duty Cycle 90 mA
 T_J Junction Temperature Range -55 to +125°C
 T_S Storage Temperature Range -55 to +125°C
 P_D Power Dissipation (derate at
 5.5mW/°C, above +85°C) 500 mW

RECOMMENDED OPERATING CONDITIONS

V⁻ Negative Supply Voltage -8.0 to -15V
 V⁺ Positive Supply Voltage +8.0 to +15V
 V_{IN} Control Input Voltage Range 0 to +5V
 T_{OP} Operating Temperature
 (A Suffix) -55 to +125°C
 (B Suffix) -25 to +85°C
 (C Suffix) 0 to +70°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V⁻ = -15V, V⁺ = +15V per channel, unless otherwise noted)

#	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
1	V _{ANALOG}	Analog Signal Range	-10		+10	V	
2	r _{DS(on)}	Switch ON Resistance		40	80	Ω	V _S = -10V V _S = +2.0V V _S = +10V V _{IN} = 0
3				45	80		
4				100	160		
5	V _{IH}	High Level Input Voltage	2.4			V	
6	V _{IL}	Low Level Input Voltage			0.8		
7	I _{IN}	Logic Input Leakage Current		0.01	0.1	μA	V _{IN} = +2.4V V _{IN} = +15V
8				0.02	0.1		
9	I _{D(OFF)}	Switch OFF Leakage Current		0.2	5.0	nA	V _D = +10V, V _S = -10V V _S = +10V, V _D = -10V V _{IN} = +2.4V
10	I _{S(OFF)}			0.4	5.0		
11	I ⁻	Negative Supply Quiescent Current		-0.3	-1.0	mA	V _{IN} = 0 or +2.4
12	I ⁺	Positive Supply Quiescent Current		0.6	2.0		
13	t _{ON}	Switch Turn-On Time		400	600	nSec	See Switching Times Test Circuit
14	t _{OFF}	Switch Turn-OFF Time		70	300		
15	O _{IRR}	OFF Isolation, Rejection Ratio	60	66		dB	f = 10 MHz R _L = 50Ω
16	C _{CCR}	Cross-Coupling Rejection Ratio		80			
17	C _d	Drain-Node Capacitance		0.3		pF	V _D = V _S = 0 f = 1MHz V _{IN} = +2.4V
18	C _s	Source-Node Capacitance		3.0			

ELECTRICAL CHARACTERISTICS (V⁻ = -15V, V⁺ = +15V, per channel unless otherwise noted)

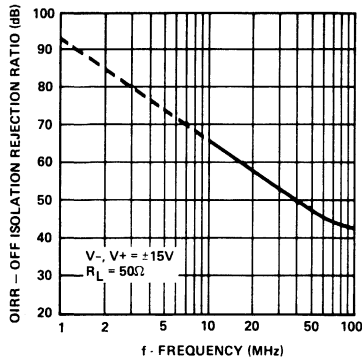
LIMITS AT TEMPERATURE EXTREMES

#	SYMBOL	PARAMETER	MAXIMUM @ T _A =					UNITS	TEST CONDITIONS
			-55°C	-25°C	+70°C	+85°C	+125°C		
1	V _{ANALOG}	Analog Signal Range	±10	±10	±10	±10	±10	V	
2	r _{DS(on)}	Switch ON Resistance	80	80	120	120	150	Ω	V _S = -10V V _S = +2.0V V _S = +10V V _{IN} = 0
3			80	80	120	120	150		
4			160	160	240	240	300		
5	I _{IN}	Logic Input Leakage Current	0.1	0.1	1.0	1.0	10	μA	V _{IN} = +2.4V V _{IN} = +15V
6			0.1	0.1	2.0	2.0	20		
7	I _{D(OFF)}	Switch OFF Leakage Current	5.0	5.0	100	100	1000	nA	V _D = +10V, V _S = -10V V _S = +10V, V _D = -10V V _{IN} = +2.4V
8	I _{S(OFF)}		5.0	5.0	100	100	1000		
9	I ⁻	Supply Quiescent Currents	-1.0	-1.0	-1.0	-1.0	-1.0	mA	V _{IN} = 0 or +2.4V
10	I ⁺		2.0	2.0	2.0	2.0	2.0		

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$, per channel, unless otherwise specified)

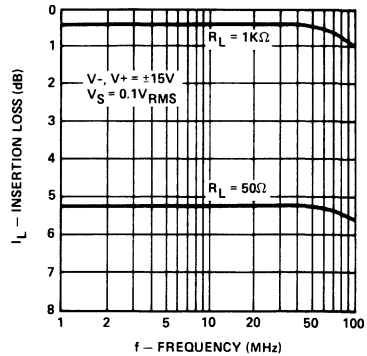
SWITCH-OFF ISOLATION REJECTION RATIO

—VS—
FREQUENCY



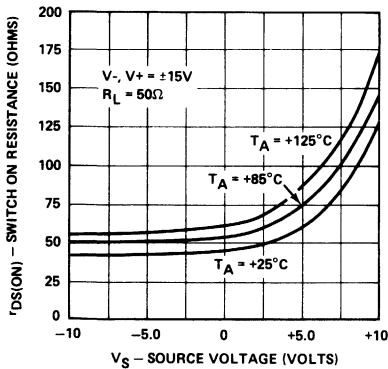
INSERTION LOSS

—VS—
FREQUENCY



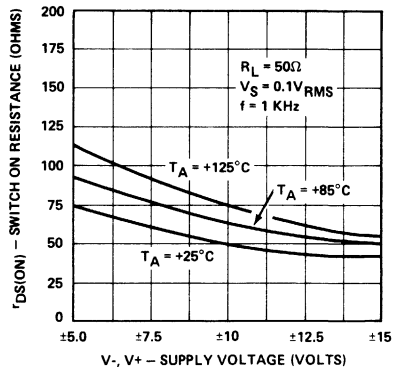
SWITCH ON RESISTANCE

—VS—
ANALOG VOLTAGE



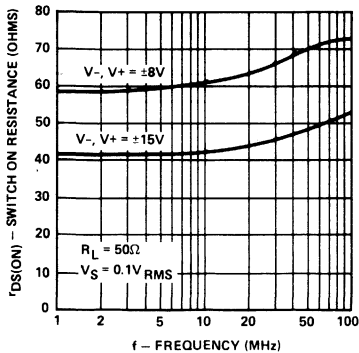
SWITCH-ON RESISTANCE

—VS—
SUPPLY VOLTAGES



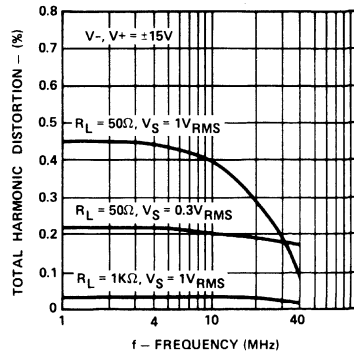
SWITCH-ON RESISTANCE

—VS—
FREQUENCY



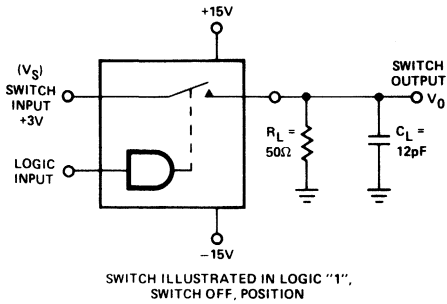
TOTAL HARMONIC DISTORTION

—VS—
FREQUENCY

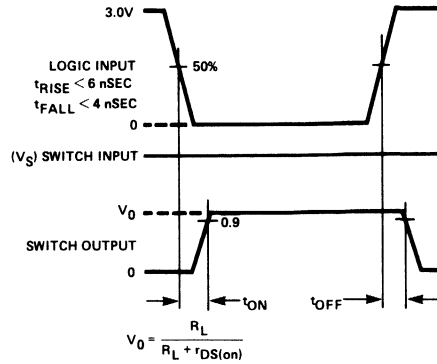


TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$, per channel, unless otherwise specified)

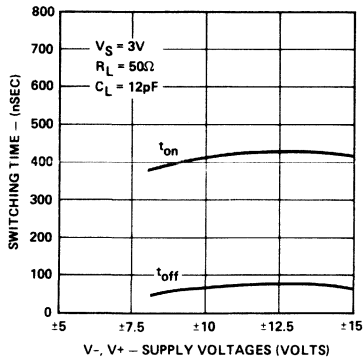
SWITCHING TIMES TEST CIRCUIT



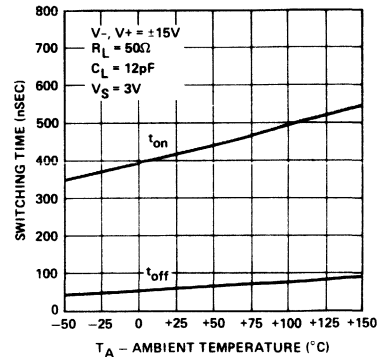
TEST WAVEFORMS



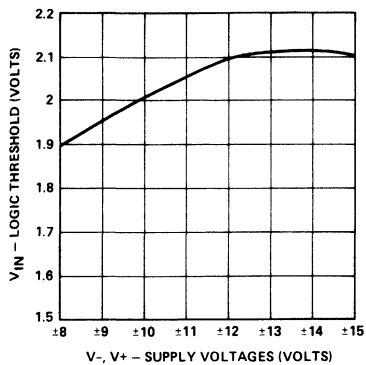
SWITCHING TIMES
—VS—
SUPPLY VOLTAGES



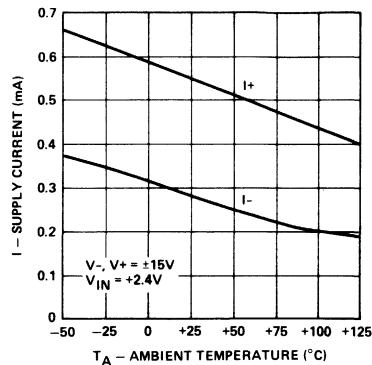
SWITCHING TIMES
—VS—
AMBIENT TEMPERATURE



LOGIC THRESHOLD
—VS—
SUPPLY VOLTAGES



SUPPLY CURRENTS
—VS—
AMBIENT TEMPERATURE



QUAD MONOLITHIC SPST CMOS/D-MOS ANALOG SWITCH

ORDERING INFORMATION

Quad SPST Switch, Logic '1' ON, Break Before Make	16-Pin Plastic DIP	20-Pin Surface Mount Package
Commercial Temp. Range	CDG211CJ	
Ext. Industrial Temp. Range		CDG211DY

FEATURES

- High OFF Isolation, 66 dB @ 10MHz
- Wide Bandwidth Switches, 0.9 x DC @ 100MHz
- Low Channel-to-Channel Cross Talk, -80 dB @ 10MHz
- TTL Compatible
- Low 'OFF' Leakage
- Industry Standard Pin-Outs

APPLICATIONS

- Glitch-Free Analog Switches
- RF & Video Switches
- Track and Hold Switches
- Sample and Hold Switches

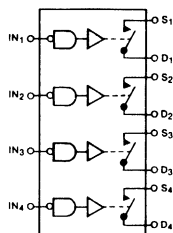
DESCRIPTION

The Topaz Semiconductor CDG211 low cost Analog Switch features TTL compatible input logic and wide-band Lateral D-MOS switches on a single chip. The on-chip reference used for TTL compatibility gives the added advantage of constant logic switching over a wide range of supply voltages and temperature without a separate power supply. Industry standard pin-out makes the CDG211 particularly suitable for replacement of existing analog switches and at the same time upgrading high frequency performance.

NOTE

All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic voltage level (V_{DD} or GND).

FUNCTIONAL BLOCK DIAGRAM

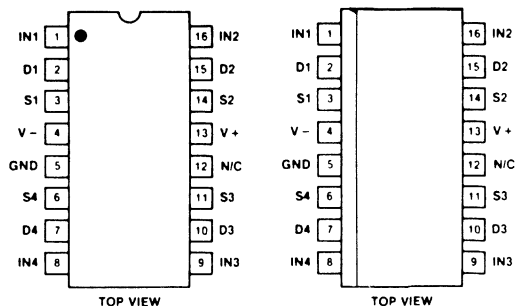


Four SPST Switches per Package
Switches shown in Logic '1' Input Position

LOGIC TABLE

Logic	Switch	
0	ON	Logic '0' \cong 0.8V
1	OFF	Logic '1' \cong 2.4V

PIN CONFIGURATIONS



CDG211CJ
(See Package 10)

CDG211DY
(See Package 21)

ABSOLUTE MAXIMUM RATINGS

V- Negative Supply Voltage -20V
 V+ Positive Supply Voltage +20V
 V_{IN} Control Input Voltage Range V+ +0.3V,
 V- -0.3V
 I_L Continuous Current, any Pin
 Except S or D 30 mA
 I_S Continuous Current, S or D 30 mA
 I_S Peak Pulsed Current, S or D,
 80μsec, 1%, Duty Cycle 90 mA
 T_S Storage Temperature Range -55 to +125°C
 P_D Power Dissipation 500mW

RECOMMENDED OPERATING CONDITIONS

V- Negative Supply Voltage -8.0 to -15V
 V+ Positive Supply Voltage +8.0 to +15V
 V_{IN} Control Input Voltage Range 0 to +5V
 V_S Analog Switch Voltage Range -10 to +10V
 T_{OP} Operating Temperature (C Suffix) 0 to +70°C
 (D Suffix) -40 to +85°C

ELECTRICAL CHARACTERISTICS (V- = -15V, V+ = +15V, per channel, unless otherwise noted, T_A = +25°C)

#	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
1	V _{ANALOG}	Analog Signal Range	-10		+10	V	
2	r _{DS(on)}	Switch ON Resistance		40	80	Ω	V _S = -10V V _S = +2.0V V _S = +10V V _{IN} = 0
3				45	80		
4				100	160		
5	V _{IH}	High Level Input Voltage	2.4			V	
6	V _{IL}	Low Level Input Voltage			0.8		
7	I _{IN}	Logic Input Leakage Current		0.01	0.1	μA	V _{IN} = +2.4V V _{IN} = +15V
8				0.02	0.1		
9	I _{D(OFF)} I _{S(OFF)}	Switch OFF Leakage Current		0.2	5.0	nA	V _D = +10V, V _S = -10V V _S = +10V, V _D = -10V V _{IN} = +2.4V
10				0.4	5.0		
11	I-	Negative Supply Quiescent Current		-0.3	-1.0	mA	V _{IN} = 0 or +2.4V
12	I+	Positive Supply Quiescent Current		0.6	2.0		
13	t _{ON}	Switch Turn-ON Time		400	600	nSec	See Switching Times Test Circuit
14	t _{OFF}	Switch Turn-OFF Time		70	300		
15	O _{IRR}	OFF Isolation, Rejection Ratio	60	66		dB	f = 10MHz R _L = 50Ω
16	C _{CRR}	Cross-Coupling Rejection Ratio		80			
17	C _d	Drain-Node Capacitance		0.3		pF	V _D = V _S = 0 f = 1MHz V _{IN} = +2.4V
18	C _s	Source-Node Capacitance		3.0			

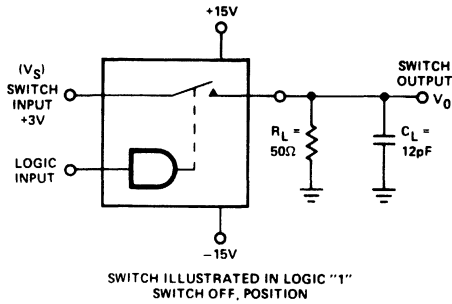
ELECTRICAL CHARACTERISTICS (V- = -15V, V+ = +15V unless otherwise noted)

Limits at Temperature Extremes

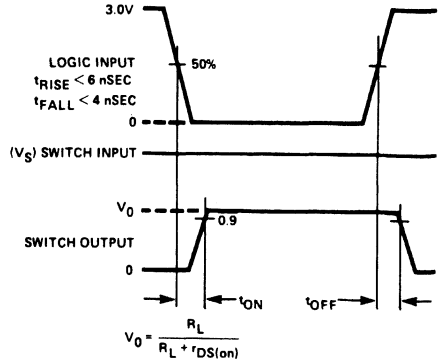
#	SYMBOL	PARAMETER	MAXIMUM @ T _A =				UNITS	TEST CONDITIONS
			-40°C	0°C	+70°C	+85°C		
1	V _{ANALOG}	Analog Signal Range	±10	±10	±10	±10	V	
2	r _{DS(on)}	Switch ON Resistance	80	80	120	120	Ω	V _S = -10V V _S = +2.0V V _S = +10V V _{IN} = 0
3			80	80	120	120		
4			160	160	240	240		
5	I _{IN}	Logic Input Leakage Current	0.1	0.1	1.0	1.0	μA	V _{IN} = +2.4V V _{IN} = +15V
6			0.1	0.1	2.0	2.0		
7	I _{D(OFF)} I _{S(OFF)}	Switch OFF Leakage Current	5.0	5.0	100	100	nA	V _D = +10V, V _S = -10V V _S = +10V, V _D = -10V V _{IN} = +2.4V
8			5.0	5.0	100	100		
9	I-	Negative Supply Quiescent Current	-1.0	-1.0	-1.0	-1.0	mA	V _{IN} = 0 or +2.4V
10	I+	Positive Supply Quiescent Current	2.0	2.0	2.0	2.0		

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$, per channel, unless otherwise specified)

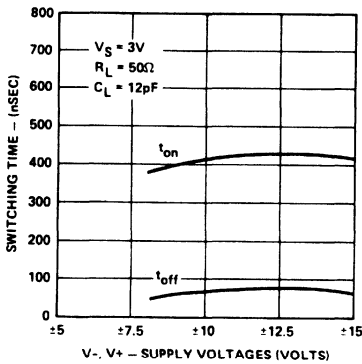
SWITCHING TIMES TEST CIRCUIT



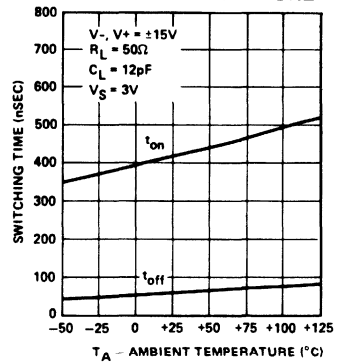
TEST WAVEFORMS



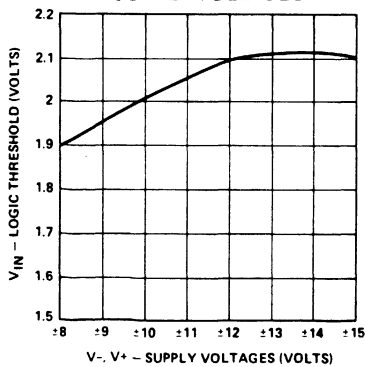
SWITCHING TIMES
—VS—
SUPPLY VOLTAGES



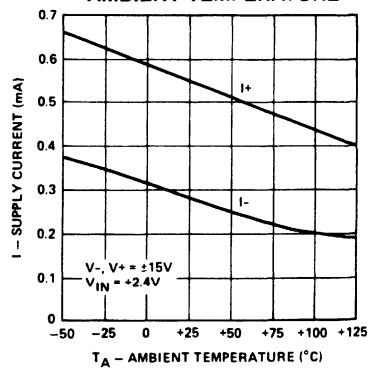
SWITCHING TIMES
—VS—
AMBIENT TEMPERATURE



LOGIC THRESHOLD
—VS—
SUPPLY VOLTAGES

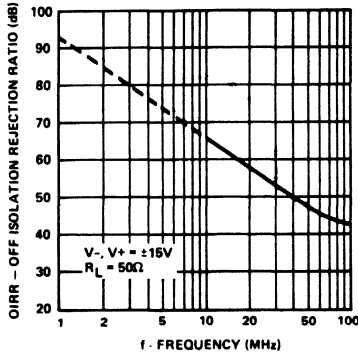


SUPPLY CURRENTS
—VS—
AMBIENT TEMPERATURE

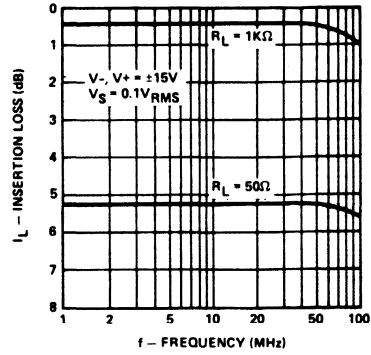


TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$, per channel, unless otherwise specified)

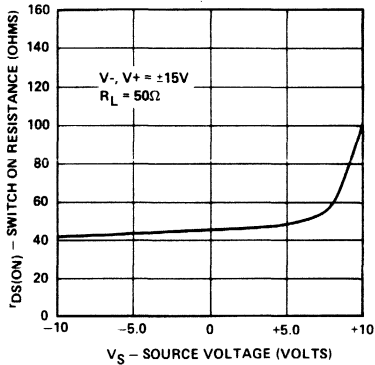
SWITCH-OFF ISOLATION REJECTION RATIO
—VS—
FREQUENCY



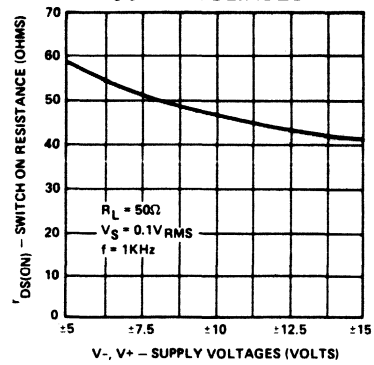
INSERTION LOSS
—VS—
FREQUENCY



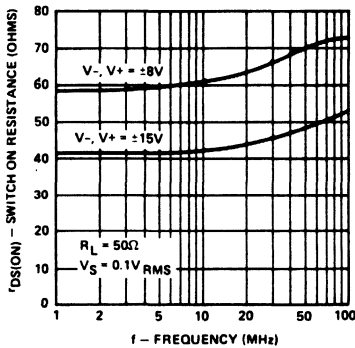
SWITCH ON RESISTANCE
—VS—
ANALOG VOLTAGE



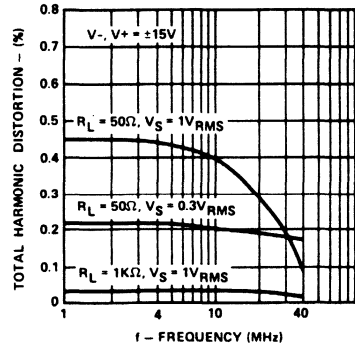
SWITCH-ON RESISTANCE
—VS—
SUPPLY VOLTAGES



SWITCH-ON RESISTANCE
—VS—
FREQUENCY



TOTAL HARMONIC DISTORTION
—VS—
FREQUENCY



QUAD MONOLITHIC SPST CMOS/D-MOS ANALOG SWITCHES

ORDERING INFORMATION

SO-8 Surface Mount Package		DIP-8 Plastic DIP		SO-8 Surface Mount Package	
CDG308DY	CDG309DY	CDG308CJ	CDG309CJ	CDG4308DJ	CDG4309DJ
CDG308DY	CDG309DY	CDG308CJ	CDG309CJ	CDG4308DJ	CDG4309DJ
Logic 1 ON	Logic 1 OFF	Logic 1 ON	Logic 1 OFF	Logic 1 ON	Logic 1 ON

FEATURES

- High Off Isolation, 68dB @ 10MHz
- Low Insertion Loss, 0.9 x DC @ 100MHz
- Low Channel-to-Channel Cross Talk, -80dB @ 10MHz
- CMOS Compatible Inputs
- Low 'OFF' Leakage
- Industry Standard Pin-Out, CDG308/309

APPLICATIONS

- Glitch-Free Analog Switches
- RF & Video Switches
- Track and Hold Switches
- Sample and Hold Switches

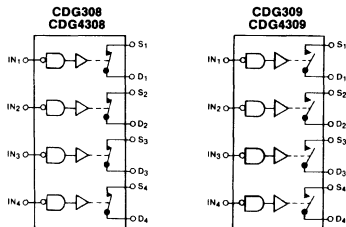
DESCRIPTION

Topaz Semiconductor CMOS/DMOS Analog Switches feature high-speed, low-power CMOS input logic and level translation circuitry and high-speed, low capacitance Lateral D-MOS switches. CMOS and Lateral D-MOS circuitry are fabricated together on a single silicon chip. The CDG4308 and CDG4309 use the same die as CDG308 and CDG309; the extra isolating pin between switch input and output increases isolation by 6dB.

NOTE

All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic voltage level (either V_{DD} or GND).

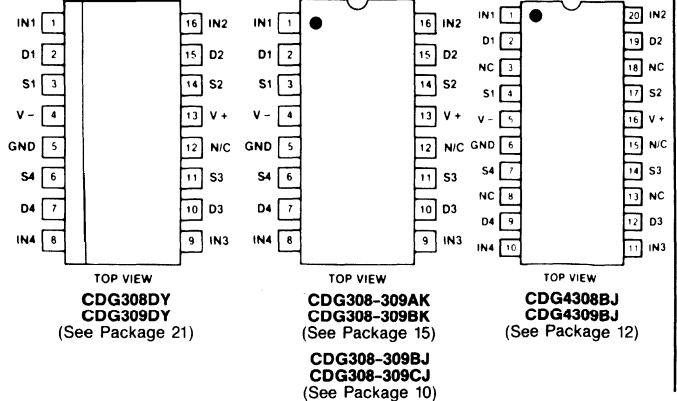
FUNCTIONAL BLOCK DIAGRAMS



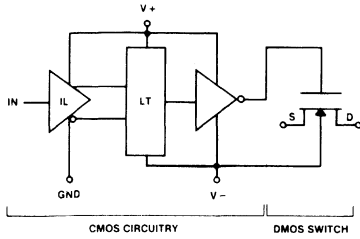
LOGIC TABLE

Logic	CDG308 CDG4308	CDG309 CDG4309
0	OFF	ON
1	ON	OFF

PIN CONFIGURATIONS



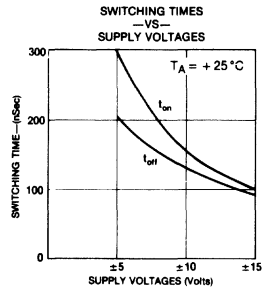
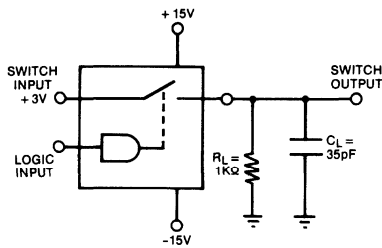
FUNCTIONAL DIAGRAM (1 of 4 channels)



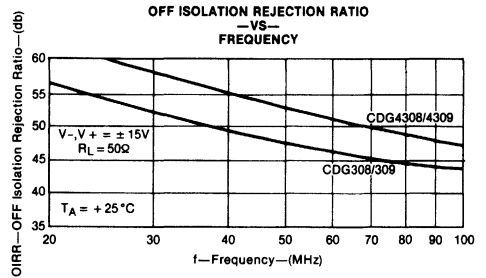
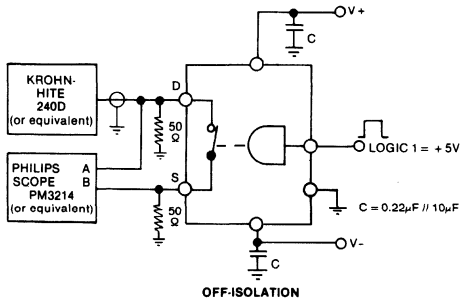
Switch Contacts:

Switches are bi-directional (Analog Input can be to Source or Drain). However, for optimum performance in Video Applications, connect Input to Source and Output to Drain.

SWITCHING TIMES TEST CIRCUIT

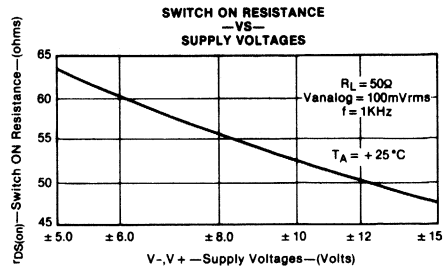
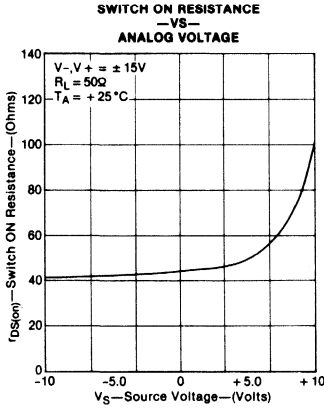


OFF ISOLATION TEST CIRCUIT

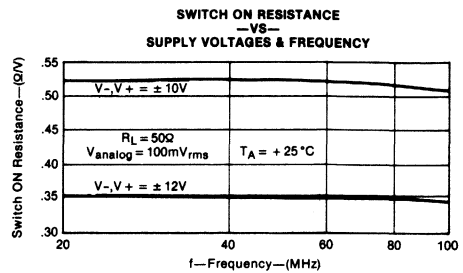
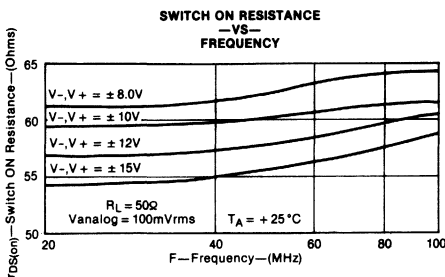
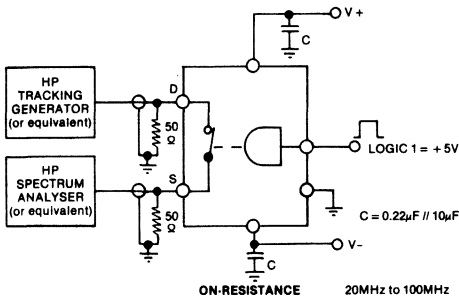


CHANNEL-TO-CHANNEL CROSSTALK TEST CIRCUIT

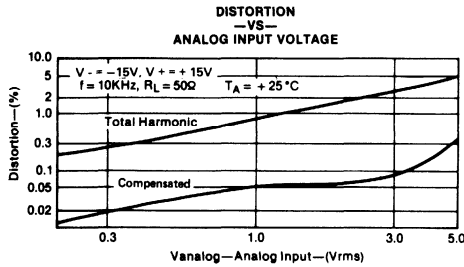
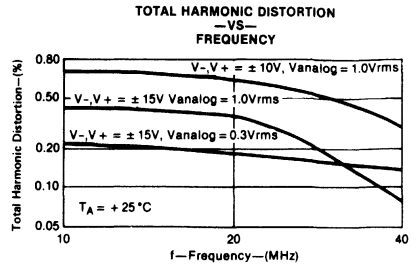
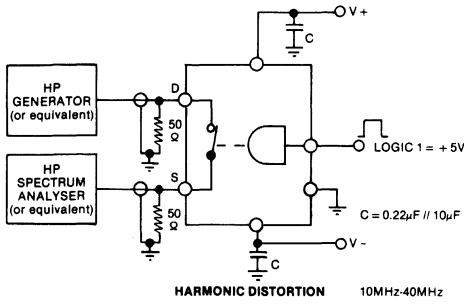
SWITCH ON RESISTANCE



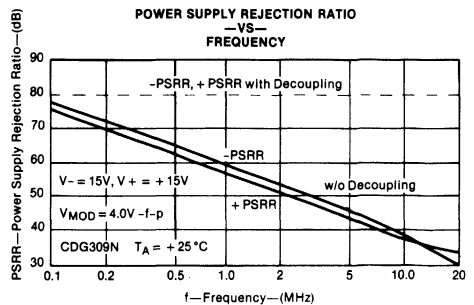
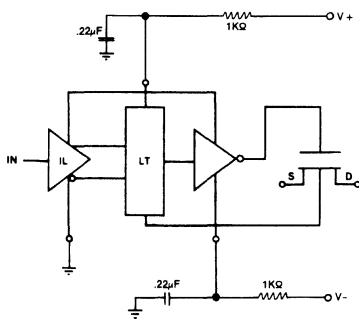
SWITCH ON RESISTANCE —VS— FREQUENCY
TEST CIRCUIT



DISTORTION —VS— FREQUENCY



**POWER SUPPLY REJECTION RATIO
POWER SUPPLY DECOUPLING CIRCUIT**

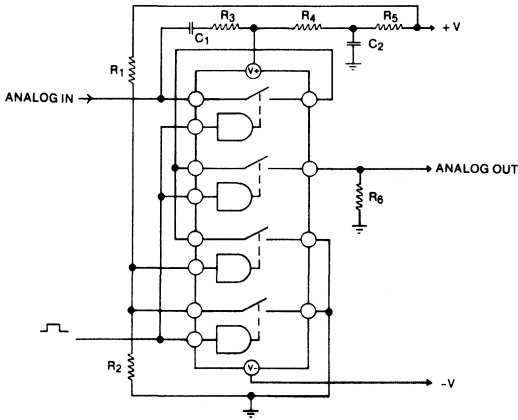


By inserting 1K ohm resistors in series with V+ and V- power supply lines and decoupling both pins at the device socket, it is possible to improve power supply rejection ratios of a video switch by 50dB at frequencies of 20MHz and higher.

APPLICATIONS

LOW DISTORTION, RAIL-TO-RAIL ANALOG SWITCH

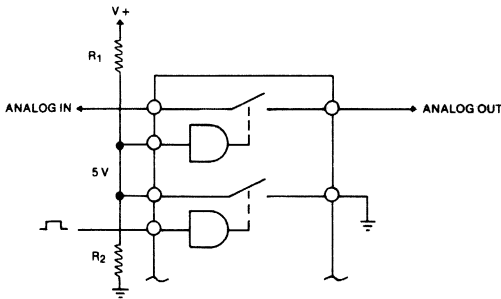
Features very low distortion for low frequency and large signal applications.



VERY LOW DISTORTION CIRCUIT FOR LOW FREQUENCY AND LARGE SIGNAL APPLICATIONS

This circuit provides very low distortion ($< 0.1\%$) and high off isolation ($> 90\text{dB}$) at signal levels equal to the supply voltage. The signal passes through a T switch configuration and at the same time is modulating the power supply. This modulation maintains a constant on resistance $r_{DS(on)}$ which in turn reduces the distortion. R_5 is for bypassing the power supply and has a typical value of 1K ohm , R_4 should be a value that can be accommodated by the signal source as load, R_3 is only necessary at loads lower than 100 ohms and should be selected during the initial design of the circuit, C_1 has to be large enough for the lowest signal to pass and C_2 will have to bypass all signals. R_1 and R_2 set up the one logic level for the control input and should be set to 5 volts .

LOGIC INVERTER



This circuit provides logic inversion with two resistors and one switch. It does not require additional logic parts. The resistors divide the supply voltage down to a 5 volt level when high and are switched to a low level via the switch. This configuration allows a single pole, single throw switch to be changed into a single pole, double throw switch.

HIGH SPEED ANALOG SWITCH

ORDERING INFORMATION



Available in Chip form.
Contact factory for Ordering Information.

FEATURES

- Ultra High OFF Isolation, > 40 dB @ 100MHz and > 25 dB @ 200 MHz
- High Speed Switching, t_{on} 40 nS and t_{off} 20 nS
- CMOS Compatible Inputs
- Low ON Resistance, < 50Ω
- Wide Bandwidth, -3 dB @ 250MHz

APPLICATIONS

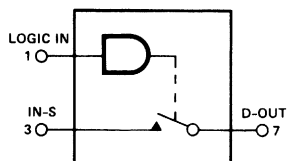
- RF & Video Switches
- High Frequency Data Acquisition
- High Frequency Multiplexers

DESCRIPTION

Topaz Semiconductor CMOS/D-MOS Analog Switches feature high-speed, low-power CMOS input logic and level translation circuitry and high speed, low capacitance Lateral D-MOS switches. CMOS and Lateral D-MOS circuitry are fabricated together on a single silicon chip.

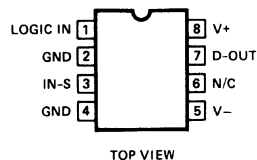
All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic level (either V_{cc} or GND).

FUNCTIONAL DIAGRAM



One SPST Switch per Package.
Switch shown in Logic "1" Input Position.
Logic '0' $\leq 1.0V$
Logic '1' $\geq 4.5V$

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

V-	Negative Supply Voltage -20V
V+	Positive Supply Voltage +20V
V _{IN}	Control Input Voltage Range V+ +0.3V, V- -0.3V
I _L	Continuous Current, any Pin Except S or D 20mA
I _S	Continuous Current, S or D 40mA
I _S	Peak Pulsed Current, S or D, 80µsec, 1%, Duty Cycle 100mA
T _J	Junction Temperature Range -55 to +125°C
T _S	Storage Temperature Range -55 to +125°C
P _D	Power Dissipation (derate at 12mW/°C, above +85°C) 500mW

RECOMMENDED OPERATING CONDITIONS

V-	Negative Supply Voltage -5 to -15V
V+	Positive Supply Voltage +5 to +15V
V _{IN}	Control Input Voltage Range 0 to +5V
T _{OP}	Operating Temperature Range	
	A Suffix -55 to +125°C
	B Suffix -25 to +85°C

ELECTRICAL CHARACTERISTICS (V₋ = -15V, V₊ = +15V unless otherwise noted, T_A = +25°C)

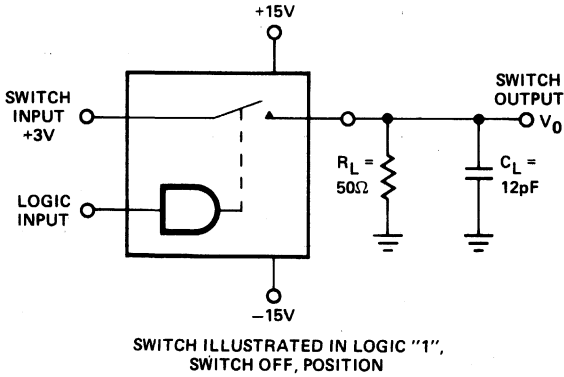
#	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
1	V _{ANALOG}	Analog Signal Range	-10		+10	V		
2	r _{DS(on)}	Switch ON Resistance		45	80	Ω	V _S = -10V	
3				50	80		V _S = +2.0V	
4				130	160		V _S = +10V	
5	V _{IH}	High Level Input Voltage	4.5	3.4		V		
6	V _{IL}	Low Level Input Voltage			1.0			
7	I _{IN}	Logic Input Leakage Current		0.01	0.1	µA	V _{IN} = +5.0V	
8				0.02	0.1		V _{IN} = +15V	
9	I _{D(OFF)}	Switch OFF Leakage Current		0.2	5.0	nA	V _D = +10V, V _S = -10, V _{IN} = 5V	
10	I _{S(OFF)}			0.2	5.0		V _S = +10V, V _D = -10, V _{IN} = 5V	
11	I ₋	Negative Supply Quiescent Current			-8.0	mA	V _{IN} = 0 or V ₊	
12	I ₊	Positive Supply Quiescent Current			8.0			
13	t _{ON}	Switch Turn-On Time		40	60	nsec	V _{IN} = 5.0V, R _L = 50Ω	
14	t _{OFF}	Switch Turn-OFF Time		20	40		C _L = 12 pF	
15	O _{IRR}	OFF Isolation Rejection Ratio	37	40		dB	R _L = 50Ω, f = 100 MHz	
16			22	25			f = 200 MHz	
17	I _L	Insertion Loss		7.8	13	dB	R _L = 50Ω, f = 200 MHz	
18	C _d	Drain-Node Capacitance		0.3			pF	V _D = 0
19	C _s	Source-Node Capacitance		3.0				V _S = 0, f = 1MHz, V _{IN} = 0

ELECTRICAL CHARACTERISTICS ($V_- = -15V, V_+ = +15V$, per channel unless otherwise noted)
LIMITS AT TEMPERATURE EXTREMES

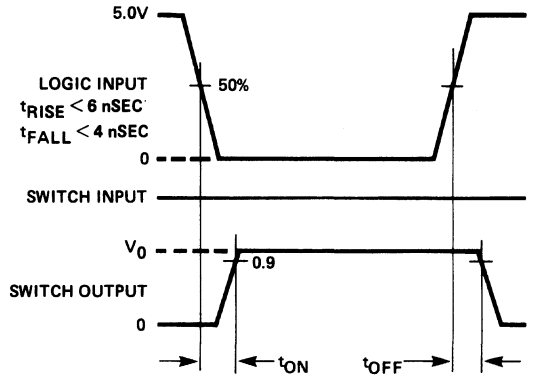
#	SYMBOL	PARAMETER	MAXIMUM @ $T_A =$				UNITS	TEST CONDITIONS
			-55°C	-25°C	+85°C	+125°C		
1	V_{ANALOG}	Analog Signal Range	±10	±10	±10	±10	V	
2	$r_{DS(on)}$	Switch On Resistance	80	80	120	150	Ω	$V_S = -10V$
3			80	80	120	150		$V_S = +2.0V$
4			160	160	240	300		$V_S = +10V$
5	I_{IN}	Logic Input Leakage Current	0.1	0.1	1.0	10	μA	$V_{IN} = +5.0V$
6			0.1	0.1	2.0	20		$V_{IN} = +15V$
7	$I_{D(OFF)}$	Switch OFF Leakage Current	5.0	5.0	200	1000	nA	$V_D = +10V, V_S = -10V, V_{IN} = 5V$
8	$I_{S(OFF)}$		5.0	5.0	200	1000		$V_S = +10V, V_D = -10V, V_{IN} = 5V$
9	I_-	Negative Supply Quiescent Current	-8.0	-8.0	-10	-10	mA	$V_{IN} = 0$ or V_+
10	I_+	Positive Supply Quiescent Current	8.0	8.0	10	10		

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25°C$ unless otherwise specified)

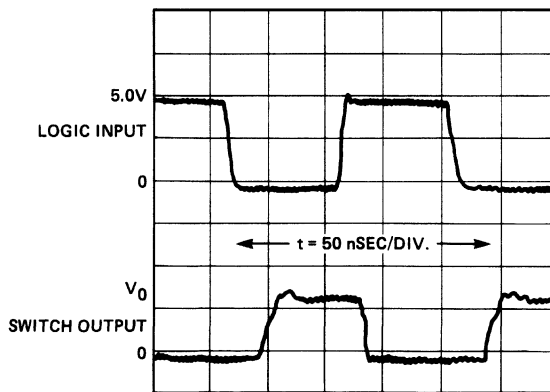
SWITCHING TIMES TEST CIRCUIT



TEST WAVEFORMS

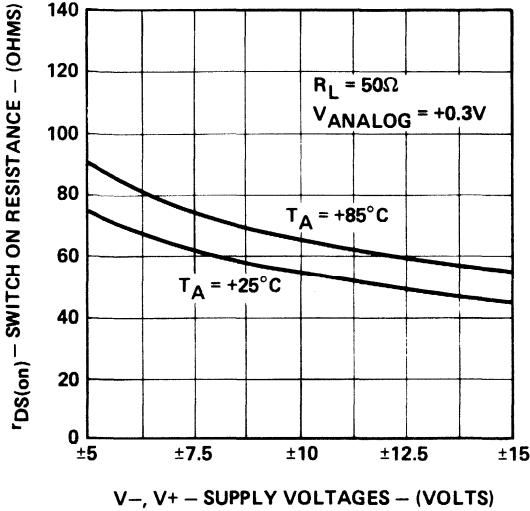


TEST RESULTS

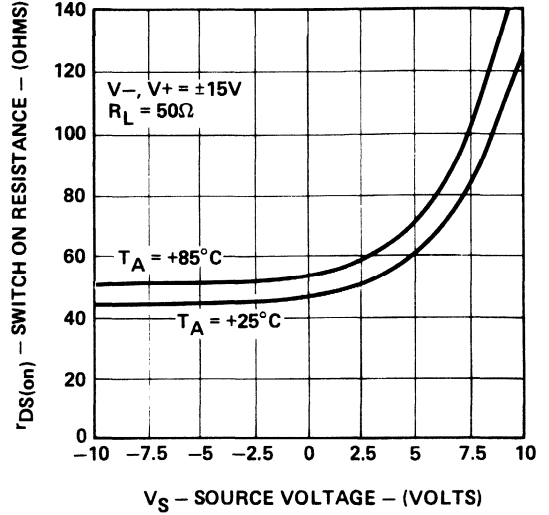


TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

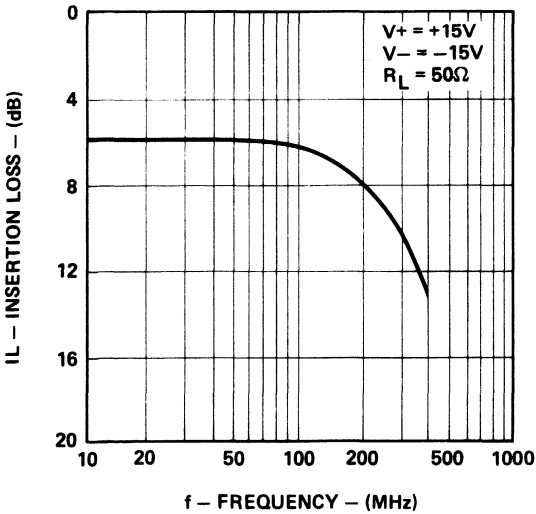
SWITCHING ON RESISTANCE
—VS—
SUPPLY VOLTAGES



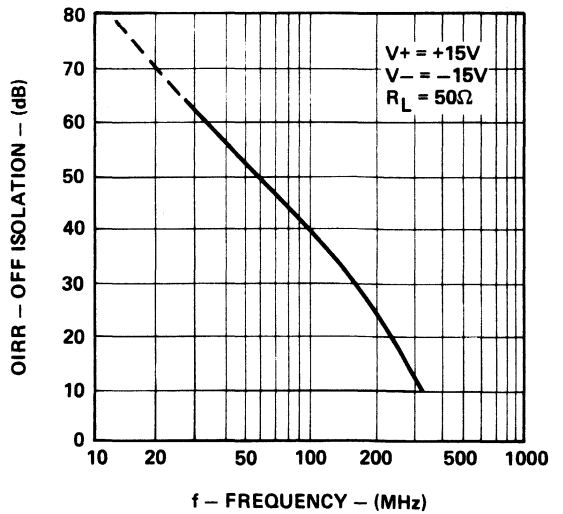
SWITCHING ON RESISTANCE
—VS—
ANALOG VOLTAGE



INSERTION LOSS
—VS—
FREQUENCY



OFF ISOLATION
—VS—
FREQUENCY



DUAL SPDT CMOS/D-MOS ANALOG SWITCHES WITH DATA LATCHES

ORDERING INFORMATION

	16-Pin Plastic DIP	SO-16 Surface Mount
Commercial Temp. Range	CDG2269CJ	CDG2269CY
Package Dimensions	See Package 10	See Package 21

FEATURES

- High OFF Isolation
- Low Channel-to-Channel Crosstalk
- Wide Bandwidth
- Analog Signal Range +10V to -10V
- Low ON Resistance, 20Ω typ.

APPLICATIONS

- RF & Video Switches
- High Speed Precision Data Acquisition
- L-PAD Digital Controlled Attenuators

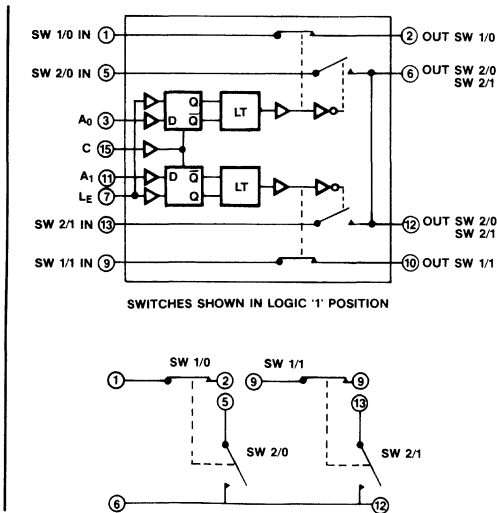
DESCRIPTION

Topaz Semiconductor CMOS/D-MOS Analog Switches feature high-speed, low-power 5 volt CMOS input logic and level translation circuitry are fabricated together on a single silicon chip. This part is designed for applications where high "off" isolation at high frequencies is needed.

NOTE

All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic level (either V_{CC} or GND).

LOGIC DIAGRAM



FUNCTION TABLE

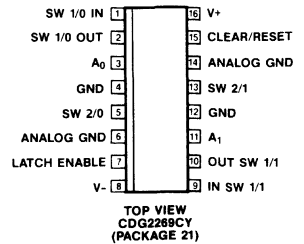
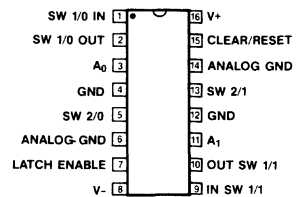
INPUT			SWITCH	
A	L_E	C	SW ₁	SW ₂
L	H	L	ON	OFF
H	H	L	OFF	ON
X	X	H	OFF	ON
L	L	L	*(1)	*(2)

X = undefined

*(1) Hold input state one setup before L_E High to Low transition. If Input state Low then Switch ON. If Input state High then Switch OFF.

*(2) SW₁ = SW₂

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

V- Negative Supply Voltage -20V
 V+ Positive Supply Voltage +20V
 V_{IN} Control Input Voltage Range V+ +0.3V, V- -0.3V
 I_L Continuous Current, any Pin except S or D ... 20mA
 I_S Continuous Current, S or D 30mA
 I_S Peak Pulsed Current, S or D, 80μsec, 1%,
 Duty Cycle 100mA
 T_J Junction Temperature Range -55 to +125°C
 T_S Storage Temperature Range -55 to +125°C
 P_D Power Dissipation 500mW

RECOMMENDED OPERATING CONDITIONS

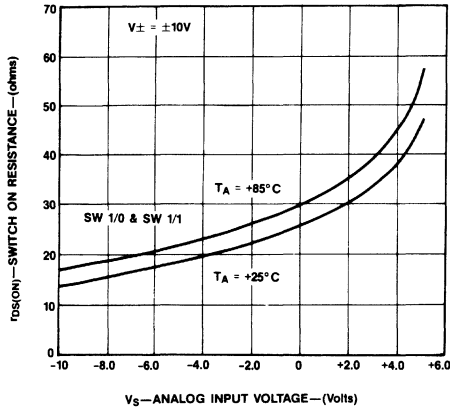
V- Negative Supply Voltage -8.0 to -15V
 V+ Positive Supply Voltage +8.0 to +15V
 V_{IN} Control Input Voltage Range 0 to +5V
 T_{OP} Operating Temperature Range
 (C Suffix) 0 to +70°C

ELECTRICAL CHARACTERISTICS (V- = -15V, V+ = +15V, per channel, unless otherwise noted, T_A = +25°C)

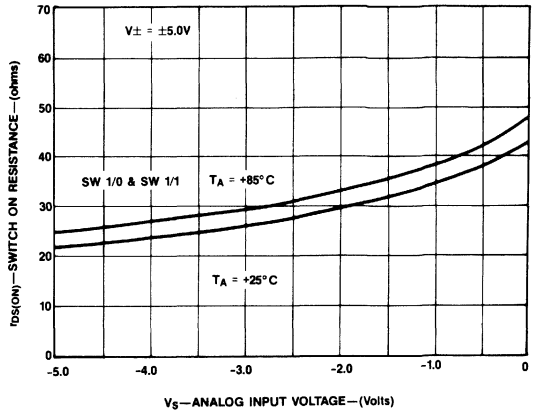
#	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
1	V _{ANALOG}	Analog Signal Range	-10		+10	V		
2	r _{DS(on)}	Channel On Resistance (Switches 2/0 & 2/1)		29	80	Ω	V _S = -10V, I _S = -1.0mA	
3				40	80		V _S = +2.0V, I _S = +1.0mA	
4				100	160		V _S = +10V, I _S = +1.0mA	
5	r _{DS(on)}	Channel On Resistance (Switches 1/0 & 1/1)		13	40	Ω	V _S = -10V, I _S = -1.0mA	
6				20	40		V _S = +2.0V, I _S = +1.0mA	
7				50	80		V _S = +10V, I _S = +1.0mA	
8	V _{IH}	Logic High Level Input Voltage	4.5	3.4		V		
9	V _{IL}	Logic Low Level Input Voltage			1.0	V		
10	I _{IN}	Logic Input Leakage Current		0.01	0.1	μA	V _{IN} = +5.0V	
11				0.02	0.1		V _{IN} = +15V	
12	I _{D(OFF)}	Switch OFF Leakage Currents	(Switches 2/0 & 2/1)		0.4	5.0	nA	V _D = +10V, V _S = -10V
13	I _{S(OFF)}				4.0	20		V _S = +10V, V _D = -10V
14	I _{D(OFF)}		(Switches 1/0 & 1/1)		0.4	5.0		V _D = +10V, V _S = -10V
15	I _{S(OFF)}				4.0	20		V _S = +10V, V _D = -10V
16	I-	Negative Supply Quiescent Current		-0.05	-0.5	μA	V _{IN} = 0 or V+	
17	I+	Positive Supply Quiescent Current		.03	0.5			
18		Propagation Delay	Data to Switch ON		180	250	nSec	
19			Data to Switch OFF		100	200		
20			Latch Enable to Sw. ON		180	250		
21			Latch Enable to Sw. OFF		140	200		
22			Clear to Switch ON		180	250		
23			Clear to Switch OFF		90	150		
24	t _S	Set Up Time	150	120				
25	t _H	Hold Time	150	90				
26	P _W	Pulse Width	50	40				
27	O _{IRR}	OFF Isolation Rejection Ratio (Switches 1/0 & 1/1)		42	45		f = 10MHz	R _L = 50Ω
28				12	15		f = 200MHz	
29		Frequency Roll-Off (Bandwidth)		1.0	3.0	dB	f = 200MHz, R _L = 50Ω	
30	I _L	Insertion Loss (Switches 1/0 & 1/1)		2.0			f = 10MHz	R _L = 50Ω
31				3.0			f = 200MHz	
32	c _d	Drain-Node Capacitance		0.6		pF	V _D = 0	f = 1MHz, V _{IN} = 0
33	c _s	Source-Node Capacitance		6.0			V _S = 0	

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

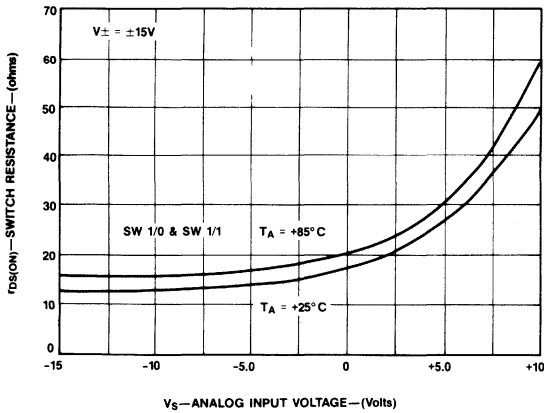
SWITCH ON RESISTANCE
—VS—
ANALOG INPUT VOLTAGE



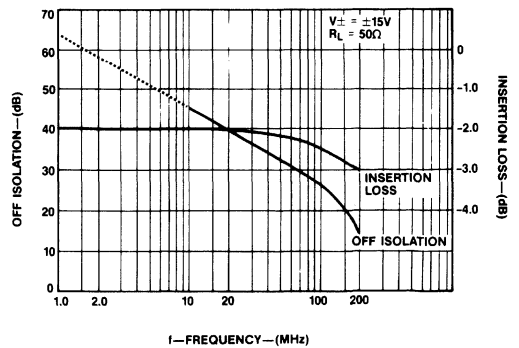
SWITCH ON RESISTANCE
—VS—
ANALOG INPUT VOLTAGE



SWITCH ON RESISTANCE
—VS—
ANALOG INPUT VOLTAGE

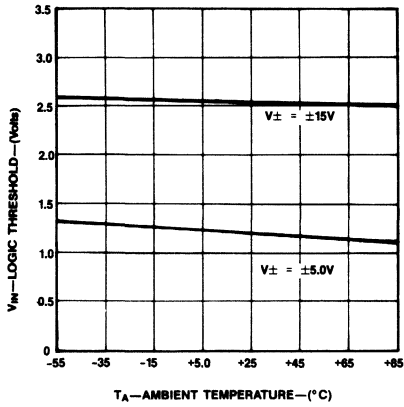


OFF ISOLATION & INSERTION LOSS
—VS—
FREQUENCY

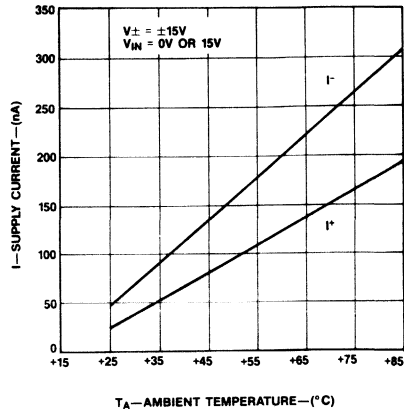


TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

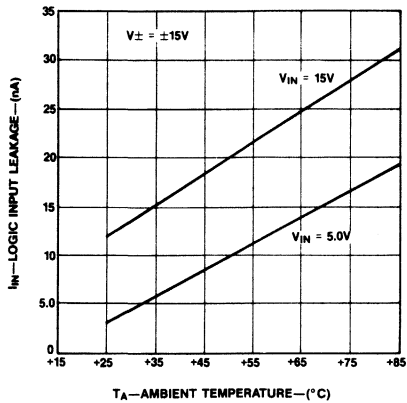
LOGIC THRESHOLD
—vs—
SUPPLY VOLTAGES & TEMPERATURE



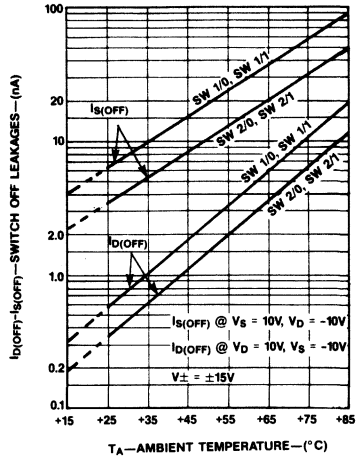
SUPPLY CURRENTS
—vs—
AMBIENT TEMPERATURE



LOGIC INPUT LEAKAGE CURRENT
—vs—
AMBIENT TEMPERATURE



SWITCH OFF LEAKAGES
—vs—
AMBIENT TEMPERATURE



6-BIT VIDEO FREQUENCY DIGITAL CONTROLLED ATTENUATOR

ORDERING INFORMATION

FEATURES

- Data Latch
- Attenuation Range of 0 to 15.75dB
- Precise Attenuation, Selectable in 0.25dB steps
- Wide Frequency Range, up to 40MHz
- Wide Power Supply Range, ± 6.0 to $\pm 15V$
- Lower Power Consumption, $0.5\mu W$ typ. with $\pm 15V$ Power Supplies

APPLICATIONS

- Video Attenuation
- Wide Band Amplifier Gain Control
- Variable Burst Generation
- IF Amplifier Attenuation
- Frequency Synthesizers

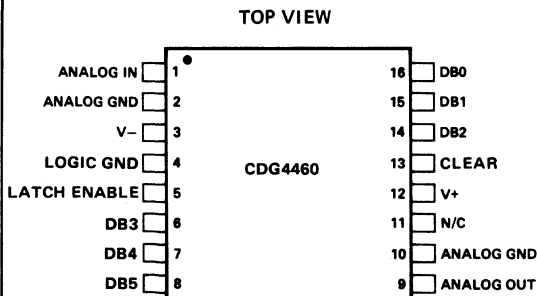
DESCRIPTION

CDG4460J remote controlled Video Attenuators feature Integrated Circuits with high OFF Isolation Lateral D-MOS FETs and low-power CMOS logic with data latches. CMOS/D-MOS ICs are mounted on ceramic substrates along with precision, trimmed resistors. A feature of this circuit is the ability to latch in the attenuator setting for easy microprocessor interfacing.

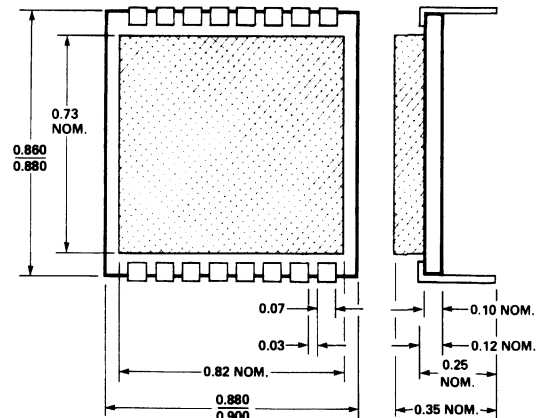
NOTE

All devices contain diodes to protect logic inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed maximum recommended logic or analog input voltages. All unused logic inputs must be connected to logic ground.

PIN CONFIGURATION

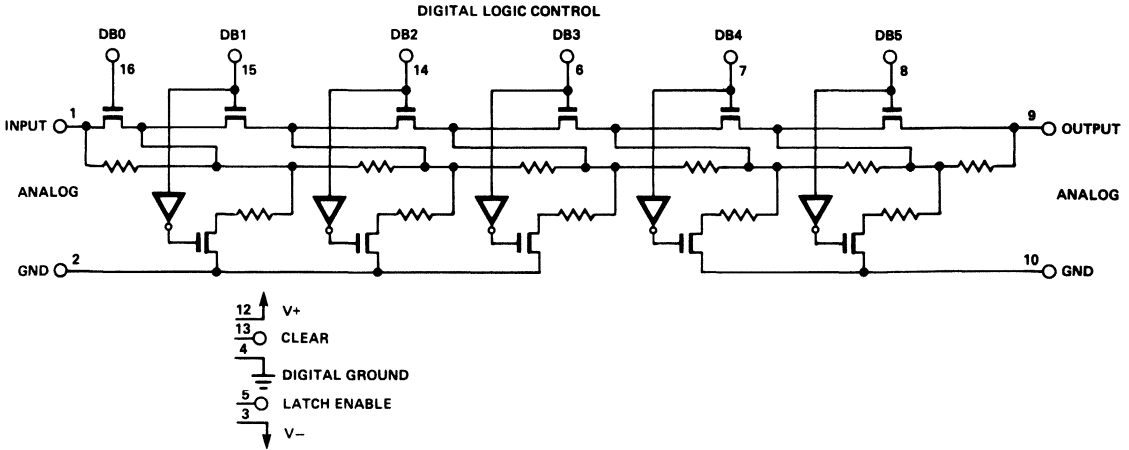


PACKAGE DIMENSIONS



ALL DIMENSIONS IN INCHES

SCHEMATIC DIAGRAM



ATTENUATOR SETTING TABLE

Note: Examples only. Added attenuation can be set to any value between 0 and 15.75dB in 0.25dB steps.

ADDED ATTENUATION (dB)	DATA BIT #—LOGIC SETTING					
	DB0	DB1	DB2	DB3	DB4	DB5
0	0	0	0	0	0	0
0.25	1	0	0	0	0	0
0.50	0	1	0	0	0	0
1.00	0	0	1	0	0	0
2.00	0	0	0	1	0	0
4.00	0	0	0	0	1	0
8.00	0	0	0	0	0	1

EXAMPLES OF OTHER ATTENUATION SETTINGS

0.75	1	1	0	0	0	0
1.75	1	1	1	0	0	0
3.75	1	1	1	1	0	0
7.75	1	1	1	1	1	0
15.25	1	0	1	1	1	1
15.75	1	1	1	1	1	1

ABSOLUTE MAXIMUM RATINGS

V-, V+	Supply Voltages	±20V
V _{IN}	Control Input Voltage Range	V- to V+
V _A	Analog Input Voltage	±4.0V
I	Continuous Current, any Pin	20mA
T _J	Junction Temperature Range	-55 to +125°C
T _s	Storage Temperature Range	-55 to +125°C
P _D	Power Dissipation	600mW

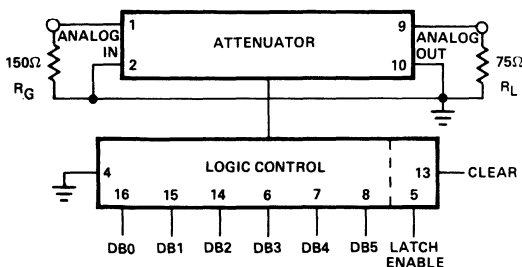
RECOMMENDED OPERATING CONDITIONS

V-, V+	Supply Voltage Ranges	±6.0V to ±15V
V _{IN}	Control Input Voltage Range	0 to +5V
V _A	Analog Input Voltage	±3.0V
T _{OP}	Operating Junction Temperature Range	-40 to +85°C

ELECTRICAL CHARACTERISTICS (V- = -15V, V+ = +15V, T_A = +25°C)

#	SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS	
1	V _{IH}	High Level Input Voltage	4.5	3.4		V		
2	V _{IL}	Low Level Input Voltage			1.0			
3	I _{IN}	Logic Input Leakage Current		0.01	0.1	µA	V _{IN} = +5.0V	
4				0.02	0.1		V _{IN} = +15V	
5	I-	Negative Supply Quiescent Current		-0.5	-100	µA	V _{IN} = 0 or V+	
6	I+	Positive Supply Quiescent Current		0.5	100			
7		Insertion Loss			6.0	dB	R _G = 150 Ω, R _L = 75 Ω Attenuation Setting=0dB	
8	t _{PD}	Propagation Delay	Data to Attn. Set		140	250	nS	V _{IN} = 5.0V
9	t _{PC}		Clear to Attn. Reset		100	220		
10	t _S	Set Up Time, Data to Latch Enable		150		nS		
11	t _H	Hold Time Latch Enable to Data OFF		150		nS		

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

LATCH ENABLE	CLEAR	ATTENUATOR
0	0	Holds data pattern already set.
x	1	Sets all data bits high-max. attenuation
1	0	Latch transparent, attenuation per setting

x = don't care, Logic '0' ≤ 1.0V, Logic '1' ≥ 4.5V

NOTES:

1. Analog Input Ground (pin 2) and Analog Output Ground (pin 10) must be connected to a common point.
2. Logic Ground (pin 4) must be isolated from Analog Ground (pins 2 & 10).

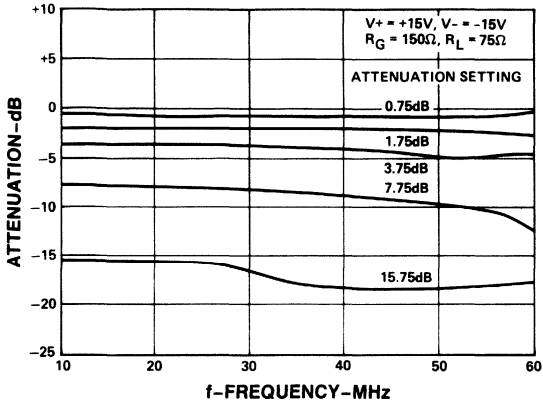
LATCH DATA

If Clear is High (Logic '1' on pin 13) all Data Bits are set to logic '1' for maximum attenuation.

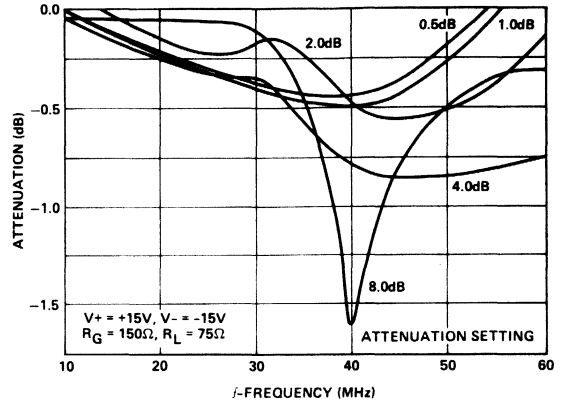
If Latch Enable is High (logic '0' on pin 5) then Latch is transparent.

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$)

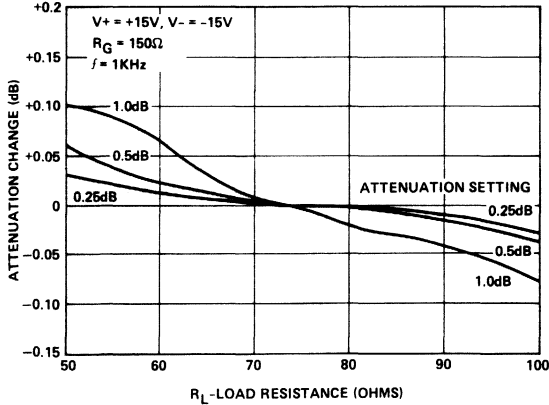
ACCUMULATED ATTENUATION
vs
FREQUENCY



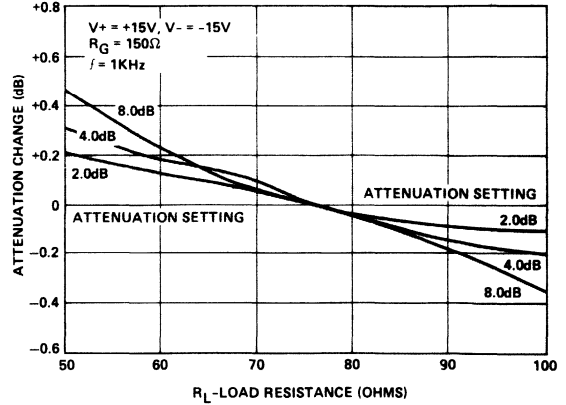
SINGLE-BIT ATTENUATION SETTING ERROR
vs
FREQUENCY



SINGLE-BIT ATTENUATION CHANGE
vs
LOAD RESISTANCE



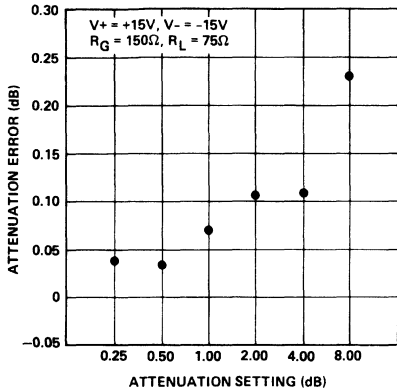
SINGLE-BIT ATTENUATION CHANGE
vs
LOAD RESISTANCE



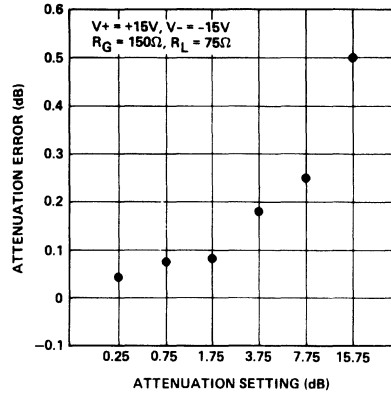
NOTE— Attenuation settings are normalized to exclude insertion loss in all curves.

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$)

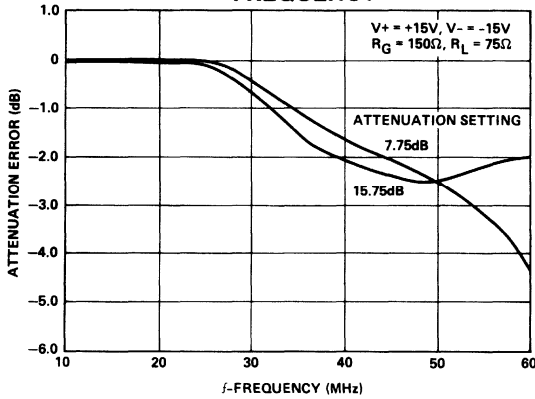
SINGLE-BIT ATTENUATION ERROR
vs
ATTENUATION SETTING



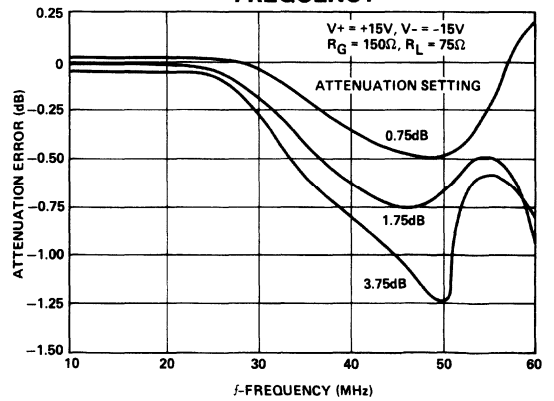
ACCUMULATED ATTENUATION ERROR
vs
ATTENUATION SETTING



ACCUMULATED ATTENUATION ERROR
vs
FREQUENCY

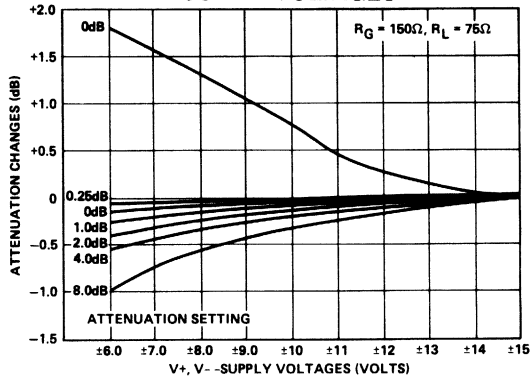


ACCUMULATED ATTENUATION ERROR
vs
FREQUENCY

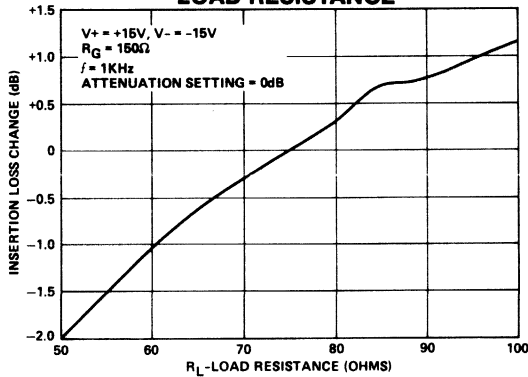


TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$)

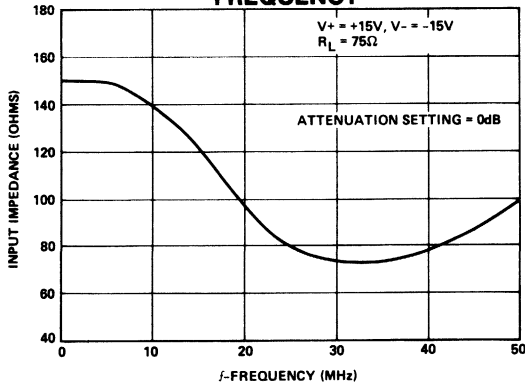
**SINGLE-BIT ATTENUATION CHANGES
VS
SUPPLY VOLTAGES**



**INSERTION LOSS CHANGE
VS
LOAD RESISTANCE**



**INPUT IMPEDANCE
VS
FREQUENCY**



8-BIT HIGH FREQUENCY DIGITAL CONTROLLED ATTENUATOR

FEATURES

- Input Voltage up to $6.0V_{RMS}$
- Attenuation Range of 0 to 127.5dB
- Precise Attenuation Selectable in 0.5dB steps
- Wide Frequency Range, up to 5MHz
- Constant Input Impedance of 650 ohms
- Wide Power Supply Range, ± 6.0 to $\pm 15V$
- Lower Power Consumption, $0.5\mu W$ typ. with $\pm 15V$ Power Supplies

APPLICATIONS

- Video Attenuation
- Digital Amplifier Gain Control
- Variable Burst Generation
- Log D/A Conversion
- Frequency Synthesizers

DESCRIPTION

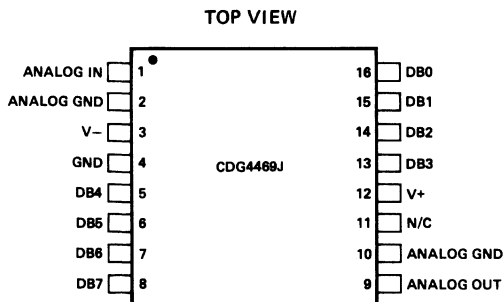
Topaz Semiconductor CMOS/D-MOS high frequency attenuators feature high-speed, low-power CMOS input logic and level translation circuitry and high speed, low capacitance Lateral D-MOS switches. CMOS and Lateral D-MOS circuitry are fabricated together on single silicon chips and mounted on hybrid circuit substrates with precision trimmed resistors.

All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic level.

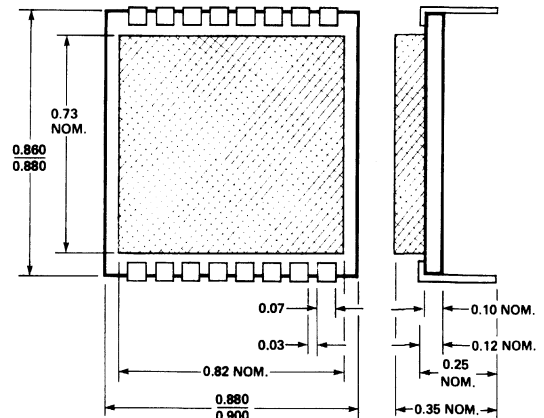
ORDERING INFORMATION



PIN CONFIGURATION

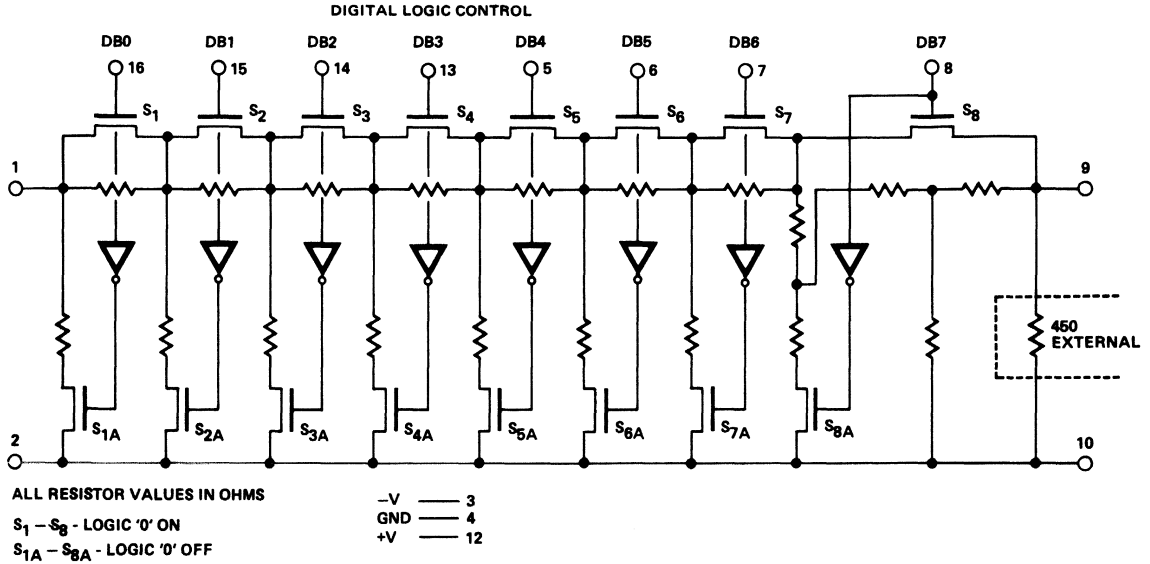


PACKAGE DIMENSIONS



ALL DIMENSIONS IN INCHES

SCHEMATIC DIAGRAM



ATTENUATOR SETTING TABLE

Note: Examples only. Added attenuation value can be set between 0 and 127.5 dB in 0.5 dB steps.

ADDED ATTENUATION (dB)	DATA BIT #—LOGIC SETTING							
	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0
0.5	1	0	0	0	0	0	0	0
1.0	0	1	0	0	0	0	0	0
2.0	0	0	1	0	0	0	0	0
4.0	0	0	0	1	0	0	0	0
8.0	0	0	0	0	1	0	0	0
16	0	0	0	0	0	1	0	0
32	0	0	0	0	0	0	1	0
64	0	0	0	0	0	0	0	1

EXAMPLES OF OTHER ATTENUATION SETTINGS

1.5	1	1	0	0	0	0	0	0
3.5	1	1	1	0	0	0	0	0
15.5	1	1	1	1	1	0	0	0
31.5	1	1	1	1	1	1	0	0
63.5	1	1	1	1	1	1	1	0
127.5	1	1	1	1	1	1	1	1

ABSOLUTE MAXIMUM RATINGS

V-, V+	Supply Voltages	±20V
V _{IN}	Control Input Voltage Range	V- to V+
V _A	Analog Input Voltage	±8.0V
I	Continuous Current, any Pin	20mA
T _J	Junction Temperature Range	-55 to +125°C
T _s	Storage Temperature Range	-55 to +125°C
P _o	Power Dissipation	600mW

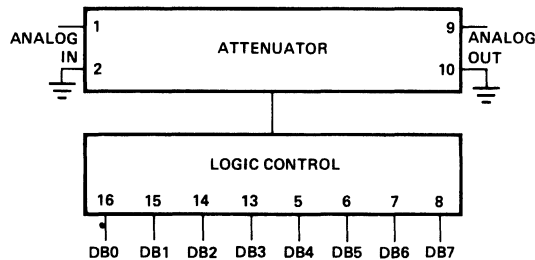
RECOMMENDED OPERATING CONDITIONS

V-, V+	Supply Voltage Ranges	±6.0V to ±15V
V _{IN}	Control Input Voltage Range	0 to +5V
V _A	Analog Input Voltage	±8.0V
T _{OP}	Operating Junction Temperature Range	-40 to +85°C

ELECTRICAL CHARACTERISTICS (V- = -15V, V+ = +15V, T_A = +25°C)

#	SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS		
1	STATIC	V _{IH}	5.0	3.4		V			
2		V _{IL}			1.0				
3		I _{IN}	Logic Input Leakage Current		0.01	0.1		µA	V _{IN} = +5.0V
4					0.02	0.1			V _{IN} = +15V
5		I-	Negative Supply Quiescent Current		-0.5	-10		µA	V _{IN} = 0 or V+
6		I+	Positive Supply Quiescent Current		0.5	10			
7	DYNAMIC			3.9	4.5	dB	R _{IN} = 650 Ω, R _L = 450 Ω Attenuation Setting=0dB		
8		t _{on}		140	250			nS	
9		t _{off}		100	220				

BLOCK DIAGRAM

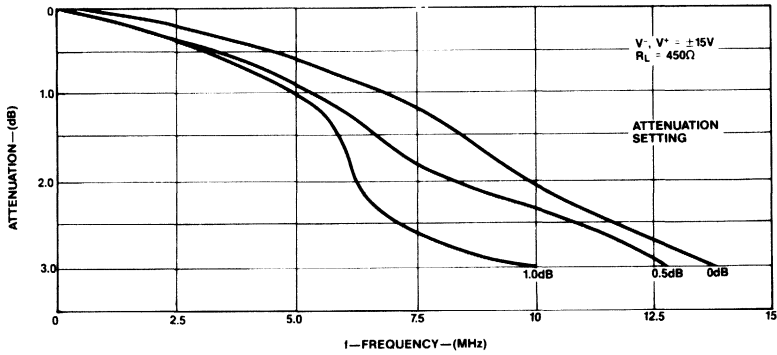


All Data Bit Pins must be connect to logic '0' or Logic '1' input according to Attenuation Setting.

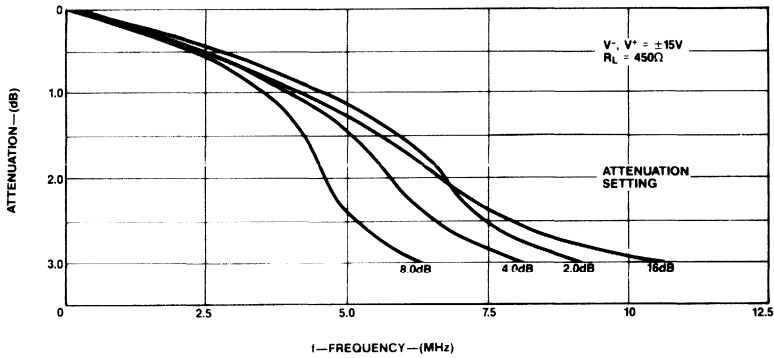
TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$)

Note: For additional performance curves refer to AN02, CDG4469J Applications Note.

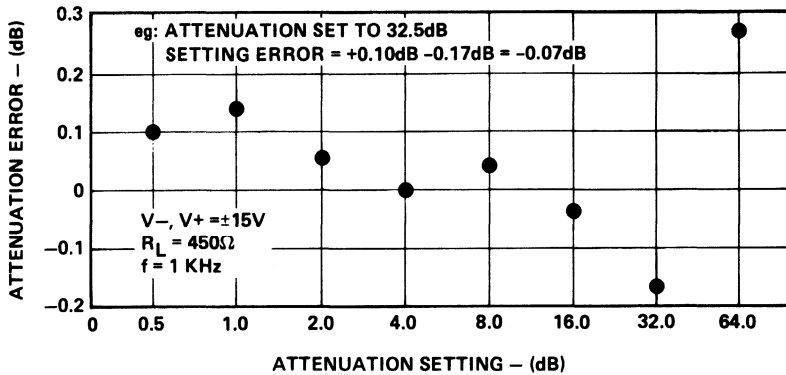
FREQUENCY RESPONSE vs ATTENUATION



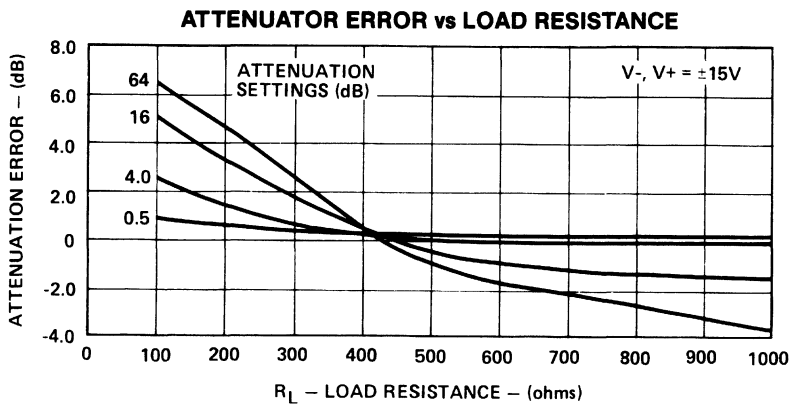
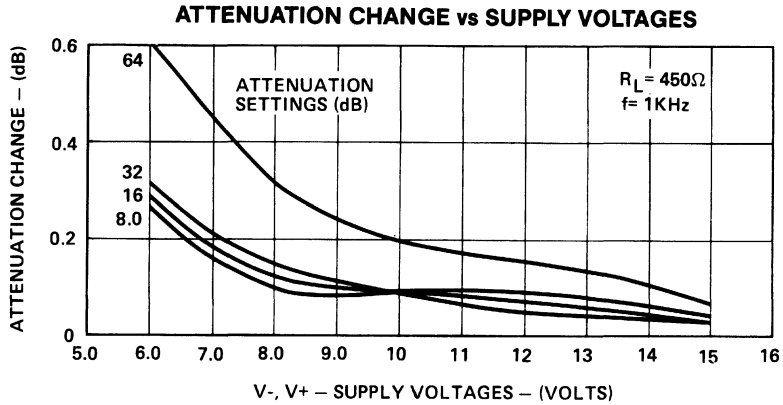
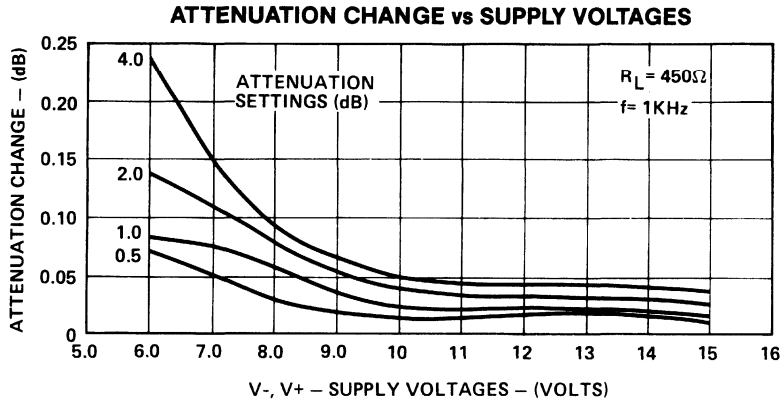
FREQUENCY RESPONSE vs ATTENUATION



ATTENUATION ERROR vs ATTENUATION SETTING

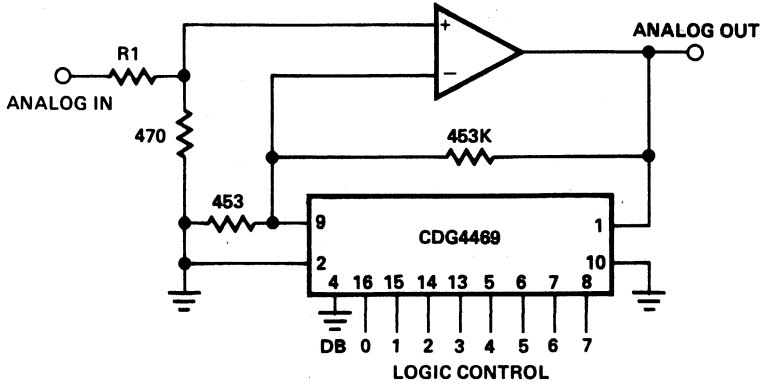


TYPICAL PERFORMANCE CHARACTERISTICS (Cont) ($T_A = +25^\circ\text{C}$)



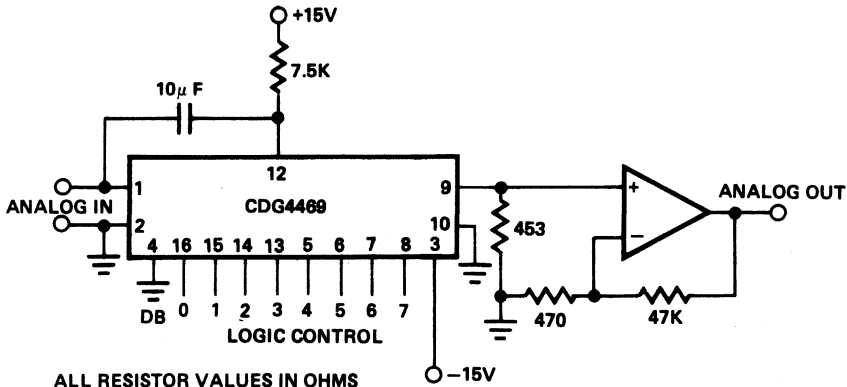
APPLICATIONS

GAIN CONTROL 0 to +60dB



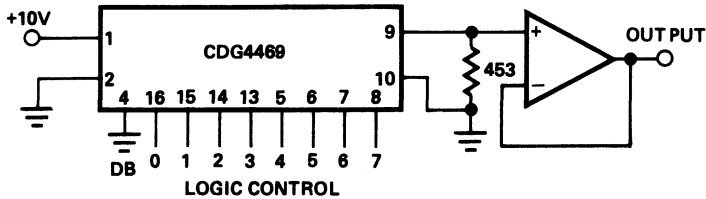
ALL RESISTOR VALUES IN OHMS
R₁ - 0 dB ADJUST

ATTENUATOR/AMPLIFIER



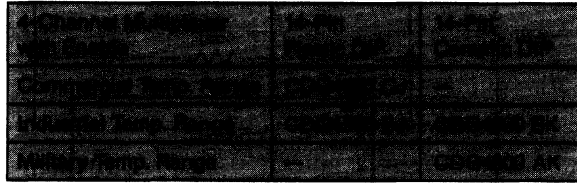
ALL RESISTOR VALUES IN OHMS
RANGE - +40 TO -87.5 dB
FREQUENCY - UP TO 500KHz

LOG D-A CONVERTER



4-CHANNEL CMOS/D-MOS HIGH-FREQUENCY MULTIPLEXER

ORDERING INFORMATION



FEATURES

- High OFF Isolation, >62dB @ 10 MHz
- Low Channel-to-Channel Crosstalk, >80dB @ 10 MHz
- 5 Volt CMOS Compatible Inputs
- Low ON Resistance, 40 Ω typ.
- Wide Bandwidth, -3.0dB @ 100 MHz
- Wide Analog Signal Range +10V to -10V
- High Speed Logic Control

DESCRIPTION

Topaz Semiconductor CMOS/D-MOS Analog Multiplexer feature high-speed, low-power 5 volt CMOS input logic and level translation circuitry and high speed, low capacitance Lateral D-MOS switches. CMOS and Lateral D-MOS circuitry are fabricated together on a single silicon chip. This part is designed for applications where high "off" isolation at high frequencies is needed. The 14 pin configuration gives a compact board layout without

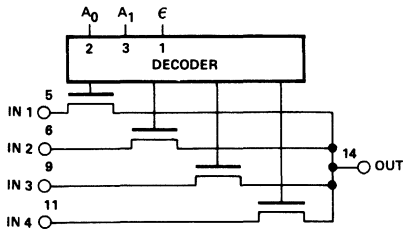
APPLICATIONS

- RF & Video Switches
- High Speed Precision Data Acquisition

impacting "off" isolation and by use of the enable allows higher levels of multiplexing.

All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic level (either V_{CC} or GND).

FUNCTION DIAGRAM

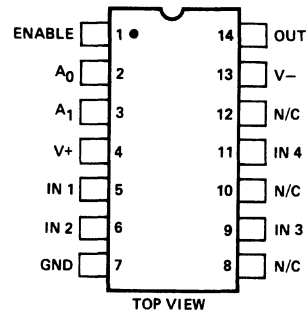


FUNCTION TABLE

ENABLE	A ₂	A ₁	CHANNEL
H	x	x	OFF
L	L	L	S ₁
L	H	L	S ₂
L	L	H	S ₃
L	H	H	S ₄

x = UNDEFINED

PIN CONFIGURATION



CDG4500AK
CDG4500BK
(See Package 14)

CDG4500BJ
CDG4500CJ
(See Package 9)

ABSOLUTE MAXIMUM RATINGS

V-	Negative Supply Voltage	-20V
V+	Positive Supply Voltage	+20V
V _{IN}	Control Input Voltage Range	V+ +0.3V, V- -0.3V
I _L	Continuous Current, any Pin except S or D	20mA
I _S	Continuous Current, S or D	30mA
I _S	Peak Pulsed Current, S or D, 80μsec, 1%, Duty Cycle	100mA
T _J	Junction Temperature Range	-55 to +125°C
T _S	Storage Temperature Range	-55 to +125°C
P _D	Power Dissipation (derate at 12mW/°C, above +85°C)	500mW

RECOMMENDED OPERATING CONDITIONS

V-	Negative Supply Voltage	-8.0 to -15V
V+	Positive Supply Voltage	+8.0 to +15V
V _{IN}	Control Input Voltage Range	0 to +5V
T _{OP}	Operating Temperature	
	(A Suffix)	-55 to +125°C
	(B Suffix)	-25 to +85°C
	(C Suffix)	0 to +70°C

ELECTRICAL CHARACTERISTICS (V- = -15V, V+ = +15V, per channel, unless otherwise noted, T_A = +25°C)

#	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
1	V _{ANALOG}	Analog Signal Range	-10		+10	V	
2	r _{DS(on)}	Channel On Resistance		40	80	Ω	V _S = -10V
3				40	80		V _S = +2.0V
4				100	160		V _S = +10V
5	V _{IH}	Logic High Level Input Voltage	4.5	3.4		V	
6	V _{IL}	Logic Low Level Input Voltage			1.0		
7	I _{IN}	Logic Input Leakage Current		0.01	0.1	μA	V _{IN} = +5.0V
8				0.02	0.1		V _{IN} = +15V
9	I _{D(OFF)}	Switch OFF Leakage Current		0.2	5.0	nA	V _D = +10V, V _S = -10V
10				0.4	5.0		V _S = +10V, V _D = -10V
11	I ₋	Negative Supply Quiescent Current	-2.0	-4.0		mA	V _{IN} = 0 or V+
12	I ₊	Positive Supply Quiescent Current	2.0	4.0			
13	t _{ON}	Switch Turn-On Time (All inputs)		150	250	nsec	V _{IN} = 5.0V
14	t _{OFF}	Switch Turn-OFF Time (All inputs)		120	220		
15	C _{CRR}	All crosstalk	62			dB	f = 10 MHz, R _L = 50Ω
16		Single Channel Crosstalk	80				
17		Frequency Roll-Off (Bandwidth)		1.0	3.0		
18	C _D	Output Node Capacitance		8.0	12.0	pF	V _D = 0
19	C _S	Input Node Capacitance		2.5	4.0		V _S = 0

ELECTRICAL CHARACTERISTICS (V- = -15V, V+ = +15V, per channel, unless otherwise noted)

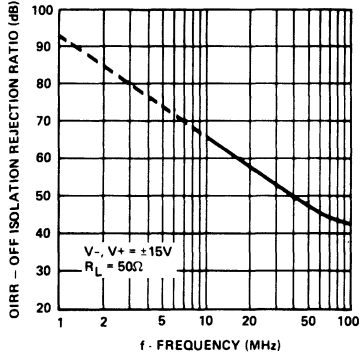
LIMITS AT TEMPERATURE EXTREMES

#	SYMBOL	PARAMETER	MAXIMUM @ T _A =					UNITS	TEST CONDITIONS
			-55°C	-25°C	+70°C	+85°C	+125°C		
1	V _{ANALOG}	Analog Signal Range	±10	±10	±10	±10	±10	V	
2	r _{DS(on)}	Channel On Resistance	80	80	120	120	150	Ω	V _S = -10V, I _S = -1.0 mA
3			80	80	120	120	150		V _S = +2.0V, I _S = +1.0 mA
4			160	160	240	240	300		V _S = +10V, I _S = -1.0 mA
5	I _{IN}	Logic Input Leakage Currents	0.1	0.1	1.0	1.0	10	μA	V _{IN} = +5.0V
6			0.1	0.1	2.0	2.0	20		V _{IN} = +15V
7	I _{D(OFF)}	Switch OFF Leakage Currents	5.0	5.0	100	100	1000	nA	V _D = +10V, V _S = -10V
8			5.0	5.0	100	100	1000		V _S = +10V, V _D = -10V
9	I ₋	Supply Quiescent Currents	-4.0	-4.0	-4.0	-4.0	-4.0	mA	V _{IN} = 0 or V+
10	I ₊		4.0	4.0	4.0	4.0	4.0		

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$, per channel, unless otherwise specified)

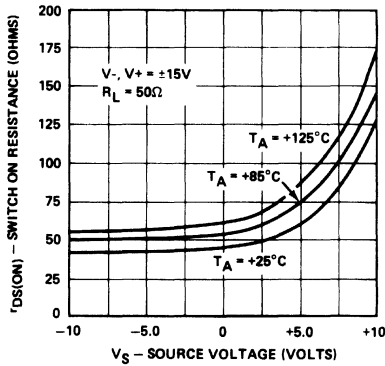
SWITCH-OFF ISOLATION REJECTION RATIO

—VS—
FREQUENCY



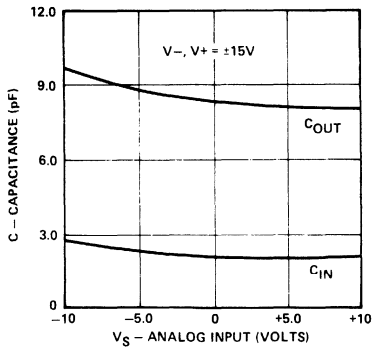
SWITCH ON RESISTANCE

—VS—
ANALOG VOLTAGE



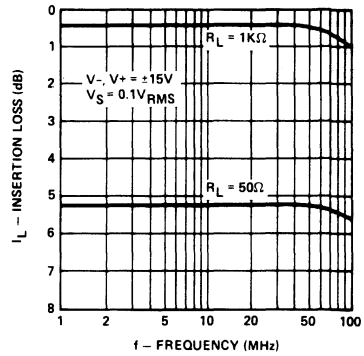
CAPACITANCE

—VS—
ANALOG INPUT VOLTAGE



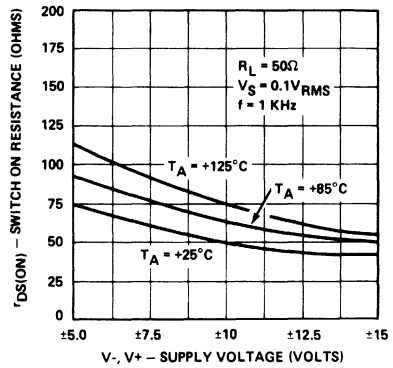
INSERTION LOSS

—VS—
FREQUENCY



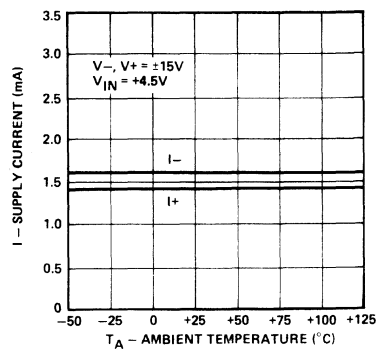
SWITCH ON RESISTANCE

—VS—
SUPPLY VOLTAGES



SUPPLY CURRENTS

—VS—
AMBIENT TEMPERATURE



TOPAZ
SEMICONDUCTOR

DUAL MONOLITHIC SPST CMOS/D-MOS T-CONFIGURATION ANALOG SWITCH

ORDERING INFORMATION

14-Pin Plastic DIP	14-Pin Plastic DIP	14-Pin Ceramic DIP
Logic '0' Input Position	CDG5341CJ	CDG5341AK
Logic '1' Input Position	CDG5341BJ	CDG5341BK
Logic '0' Input Position	—	CDG5341AK

FEATURES

- Ultra High OFF Isolation, > 80 dB @ 10MHz
- Low Channel-to-Channel Crosstalk, > 80 dB @ 10MHz
- CMOS Compatible Inputs
- Low ON Resistance, <110Ω
- Wide Bandwidth, -1.0dB @ 50MHz

APPLICATIONS

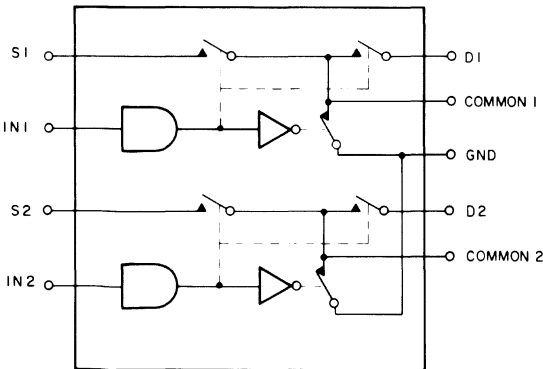
- RF & Video Switches
- Data Acquisition

DESCRIPTION

Topaz Semiconductor CMOS/D-MOS Analog Switches feature high-speed, low-power 5V CMOS input logic and level translation circuitry and high speed, low capacitance Lateral D-MOS switches. CMOS and Lateral D-MOS circuitry are fabricated together on a single silicon chip.

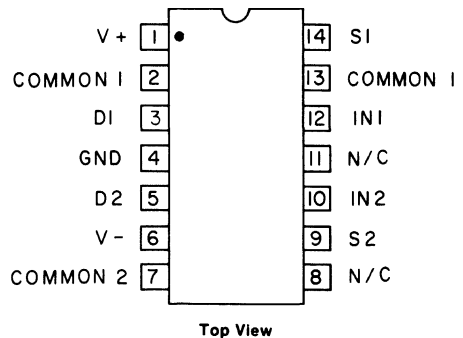
All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic level (either V_{cc} or GND).

FUNCTIONAL BLOCK DIAGRAM



Two SPST 'T' Switches per Package.
Switches shown in Logic '0' Input Position.
Compensation Networks can be connected to Common 1 and Common 2.

PIN CONFIGURATION

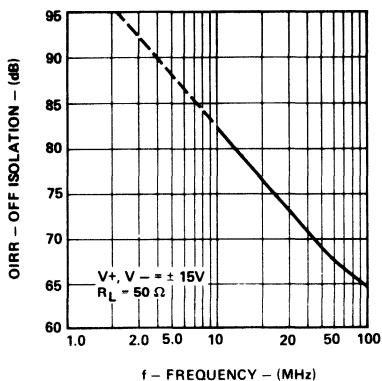


CDG5341AK
CDG5341BK
(See Package 14)

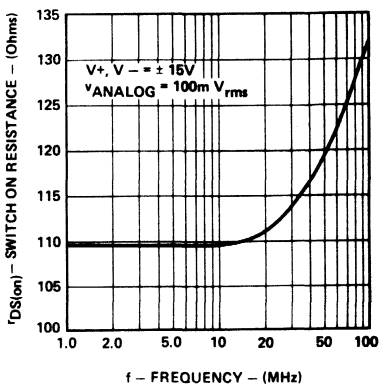
CDG5341BJ
CDG5341CJ
(See Package 9)

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

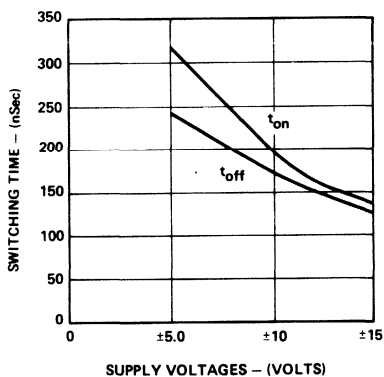
OFF ISOLATION REJECTION RATIO
—VS—
FREQUENCY



SWITCH ON RESISTANCE
—VS—
FREQUENCY



SWITCHING TIMES
—VS—
SUPPLY VOLTAGES



ABSOLUTE MAXIMUM RATINGS

V⁻ Negative Supply Voltage -20V
 V⁺ Positive Supply Voltage +20V
 V_{IN} Control Input Voltage Range V⁺ +0.3V,
 V⁻ -0.3V

I_L Continuous Current, any Pin
 Except S or D 20 mA
 I_S Continuous Current, S or D 30 mA
 I_S Peak Pulsed Current, S or D,
 80μsec, 1%, Duty Cycle 100 mA
 T_J Junction Temperature Range -55 to +125°C
 T_S Storage Temperature Range -55 to +125°C
 P_D Power Dissipation (derate at
 12mW/°C, above +85°C) 500 mW

RECOMMENDED OPERATING CONDITIONS

V⁻ Negative Supply Voltage -8.0 to -15V
 V⁺ Positive Supply Voltage +8.0 to +15V
 V_{IN} Control Input Voltage Range 0 to +5V
 V_S Analog Switch Voltage Range -10 to +10V
 T_{OP} Operating Temperature
 (A Suffix) -55 to +125°C
 (B Suffix) -25 to +85°C
 (C Suffix) 0 to +70°C

ELECTRICAL CHARACTERISTICS (V⁻ = -15V, V⁺ = +15V per channel, unless otherwise noted, T_A = +25°C)

#	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
1	V _{ANALOG}	Analog Signal Range	-10		+10	V	
2	r _{DS(on)}	Switch ON Resistance		100	160	Ω	V _S = -10V, I _S = -1.0 mA
3				110	160		V _S = +2.0V, I _S = +1.0 mA
4				200	320		V _S = +10V, I _S = -1.0 mA
5	V _{IH}	High Level Input Voltage	4.5	3.4		V	
6	V _{IL}	Low Level Input Voltage			1.0		
7	I _{IN}	Logic Input Leakage Current		0.01	0.1	μA	V _{IN} = +5.0V
8				0.02	0.1		V _{IN} = +15V
9	I _{D(OFF)}	Switch OFF Leakage Current		0.2	5.0	nA	V _D = +10V, V _S = -10V
10	I _{S(OFF)}			0.4	5.0		V _S = +10V, V _D = -10V
11	I ⁻		Negative Supply Quiescent Current	-0.1	-0.5		μA
12	I ⁺	Positive Supply Quiescent Current	0.1	0.5			
13	t _{ON}	Switch Turn-On Time		150	250	nsec	V _{IN} = 5.0V
14	t _{OFF}	Switch Turn-OFF Time		120	220		
15	O _{IRR}	OFF Isolation, Rejection Ratio	80			dB	f = 10 MHz, R _L = 50Ω
16	C _{CRR}	Cross-Coupling Rejection Ratio	80				f = 10 MHz, R _L = 50Ω
17		Frequency Roll-Off (Bandwidth)		1.0	3.0	dB	f = 50 MHz, R _L = 50Ω
18	C _d	Drain-Node Capacitance		0.3			pF
19	C _s	Source-Node Capacitance		3.0		V _S = 0	

ELECTRICAL CHARACTERISTICS (V⁻ = -15V, V⁺ = +15V, per channel)

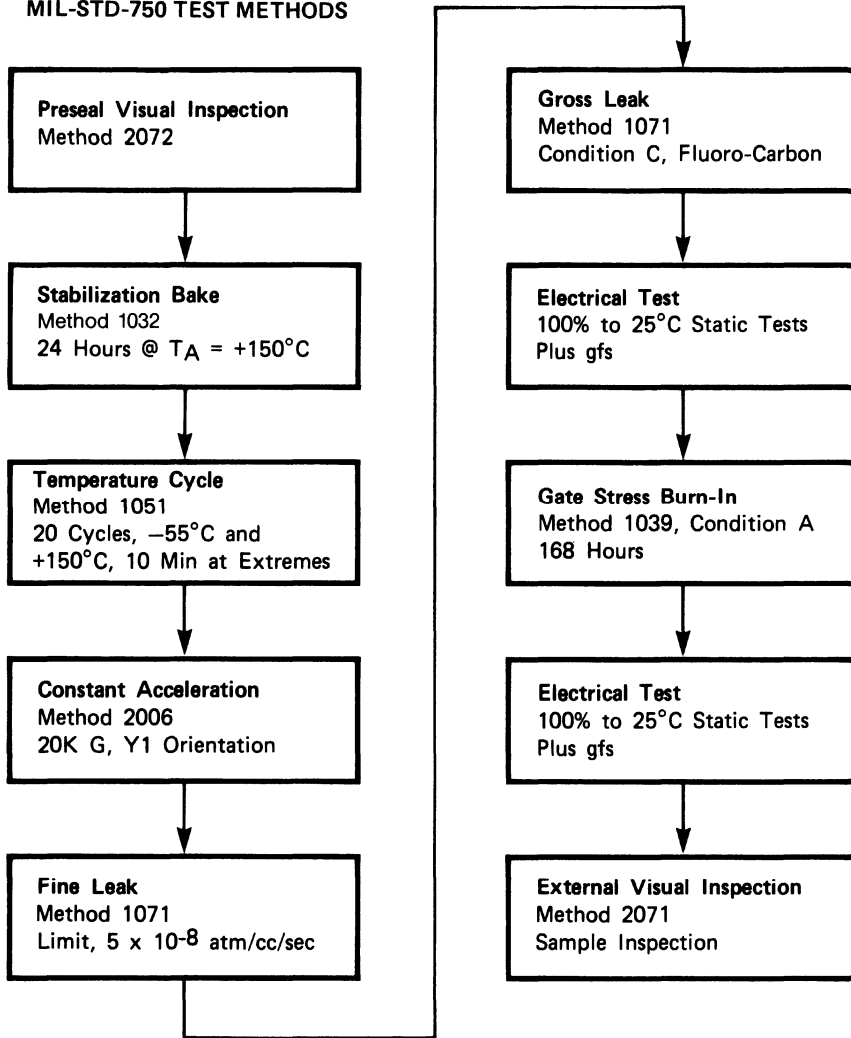
LIMITS AT TEMPERATURE EXTREMES

#	SYMBOL	PARAMETER	MAXIMUM @ T _A =					UNITS	TEST CONDITIONS
			-55°C	-25°C	70°C	+85°C	+125°C		
1	V _{ANALOG}	Analog Signal Range	±10	±10	±10	±10	±10	V	
2	r _{DS(on)}	Switch On Resistance	160	160	240	240	300	Ω	V _S = -10V, I _S = -1.0 mA
3			160	160	240	240	300		V _S = +2.0V, I _S = +1.0 mA
4			320	320	480	480	600		V _S = +10V, I _S = -1.0 mA
5	I _{IN}	Logic Input Leakage Current	0.1	0.1	1.0	1.0	10	μA	V _{IN} = +5.0V
6			0.1	0.1	2.0	2.0	20		V _{IN} = +15V
7	I _{D(OFF)}	Switch OFF Leakage Current	5.0	5.0	100	100	1000	nA	V _D = +10V, V _S = -10V
8	I _{S(OFF)}		5.0	5.0	100	100	1000		V _S = +10V, V _D = -10V
9	I ⁻	Supply Quiescent Currents	-0.5	-0.5	-20	-20	-100	μA	V _{IN} = 0 or V ⁺
10	I ⁺		0.5	0.5	20	20	100		

SECTION 3

	PAGE(S)
M+ PRODUCT ENHANCEMENT FLOW (JANTX EQUIV.)	3-2
PRODUCT SELECTOR GUIDES	
N-Channel, Enhancement-Mode, Lateral D-MOS	3-5
N-Channel, Depletion-Mode, Lateral D-MOS	3-5
N-Channel, Enhancement-Mode, Vertical D-MOS	3-4
P-Channel, Enhancement-Mode, Vertical D-MOS	3-3
 LATERAL & VERTICAL D-MOS FET SUBSTITUTION GUIDE	 3-6 to 3-23
 J-FET SUBSTITUTION GUIDE	 3-24, 3-25
 PRODUCT DATA SHEETS	 3-26 to 3-160

MIL-STD-750 TEST METHODS



NOTES:

1. Device mark after seal and prior to first electrical test.
2. Applicable to TO-18, TO-39 and TO-72 hermetic packages.
3. Off Shore build, US test and Burn-In and QC inspection.
4. All devices are shipped with shorting rings on leads.
5. All devices are shipped in bulk, packed in anti-static bags.

ORDERING INFORMATION:

To order standard catalog parts with M+ Product Enhancement, add /M to standard part number. eg: SD215DE/M

P-CHANNEL ENHANCEMENT-MODE VERTICAL D-MOSFETS

BV _{DES} (Volts) MIN	r _{DS(ON)} (ohms) MAX	Single T0-18 Hermetic	Single T0-39 Hermetic	Single T0-92 Plastic	Single T0-92R Plastic	Single T0-237 Plastic	Quad T0-237 Plastic	Octal 14-Pin DIP Plastic	Surface Mount Single SOT-89
		-400	700			SD2204BD			
	75			VP0540N3	CF				
-300	600							AP0130NA	
-200	600							AP0120NA	
-100	5.0	SD2107DD	SD2107HD	SD2107BD		SD2107AD	CF	CF	
				VP1008L		VP1008M			
-90	8.0			VP0109N3					
-80	5.0			VP0808L		VP0808M			
-60	8.0			VP0106N3					
-40	8.0			VP0104N3					

CF - Contact Factory

N-CHANNEL ENHANCEMENT-MODE VERTICAL D-MOS FETS

BV _{DS} (Volts) MIN	r _{DS(on)} (ohms) MAX	Single	Single	Single	Single	Single	Quad	Octal	Surface Mount Single SOT-89
		T0-18 Hermetic	T0-39 Hermetic	T0-92 Plastic	T0-92R Plastic	T0-237 Plastic	14-Pin DIP Plastic	18-Pin DIP Plastic	
600	60			SD1500BD					SD1500CY
550				SD1501BD					
450	700	SD1200DD							
	35	SD1100DD	SD1100HD						
400	500	SD1201DD		SD1201BD					
	350							AN0140NA	
	25	SD1101DD	SD1101HD	SD1101BD					
300	300							AN0130NA	
250	10	SD1102DD	SD1102BD						
240	10			VN2410L		VN2410M			
200	300							AN0120NA	
	250			SD1202BD					
	28				SD1122BD				
	10	SD1113DD	SD1113HD	SD1113BD					
	7.0	SD1112DD	SD1112HD	SD1112BD					
100	100							AN0110NA	
	4.0	SD1107DD	SD1107HD	SD1107BD			SD1107N		
	3.0			TN0110N3					
	2.5		CF			CF			
	0.6		2N6782						
90	3.0			SD3300HD	SD3300BD	SD3300AD			
60	7.5			VN0109N3					
	5.5			VN2222LL		VN2222LM			
	5.0	SD1106DD		2N7000	BS170	SD1106AD		VQ1000J	
				VN0610LL		VN10LM			
				VN10KN3					
	4.0			SD1127BD					
	3.0			TN0106N3					
				VN0106N3					
	2.5	SD1117DD	SD1117HD	SD1117BD		CF	SD1117N		
				SD1137BD					
0.6		2N6781							
0.4		SD3301HD	SD3301BD		SD3301AD				
40	3.0			VN0104N3					

CF - Contact Factory

N-CHANNEL ENHANCEMENT-MODE LATERAL D-MOS FETS

BV _{DSX} (Volts) MIN	BV _{SDX} (Volts) MIN	r _{DS(on)} (ohms) MAX	SINGLE T0-39 Hermetic	SINGLE T0-52+ Hermetic	SINGLE T0-72 Hermetic	SINGLE T0-92 Plastic	DUAL T0-78 Hermetic	QUAD 14/16-Pin Dip	Surface Mount Packages			
									QUAD S0-14	SINGLE S0T-89	SINGLE S0T-143	
100	0.5	10	SD221HD									
60	0.5	9.0	SD220HD									
30	10	90			SD211ADE*							
		70			SD210DE							
						2N7104						
						SD211DE*						SST211*
					2N7105*							
		0.5	80				TZ400BD*		SD5200N*			
		70						SD5100N*				
25	20	6.0			SD219DE*							
	15				SD217DE*							
	0.5	130				SD304DE*						
		70			SD200DC							
						SD201DC*						
						SD204HD						
		6.0			SD205HD*							
20	20	90			SD215ADE*							
		70			SD214DE							
						2N7108			SD5000N*	SD5400CY*		
						SD215DE*						SST215*
						2N7109*						
		0.5	100			SD306DE*						
			80		SD303DC*							
			50		SD202DC							
					SD203DC*							
			20				TZ404BD*				TZ404CY*	
15	15	70						SD5002N*	SD5402CY*			
	0.5	80				TZ402BD*						
		70						SD5101N*				
		60					TZ403BD*					
10	10	70			SD212DE		SD411HD*					
					2N7106							
					SD213DE*				SD5001N*	SD5401CY*		SST213*
					2N7107*							

* - Gate Protective Diode(s) + - 4-Lead TO-52 Package CF - Contact Factory

N-CHANNEL DEPLETION-MODE LATERAL D-MOS FETS

BV _{DSX} (Volts) MIN	BV _{SDX} (Volts) MIN	r _{DS(on)} (ohms) MAX	Single T0-39 Hermetic	Single T0-52+ Hermetic	Single T0-72 Hermetic	Single T0-92 Plastic	Dual T0-78 Hermetic	Quad 16-Pin DIP Plastic	Dual S0-8 Surface Mount
20	10	75			SD2200DE*				
		150			SD2100DE*		TZ5911HD*	SD5501N*	TZ5911CY*

* - Gate Protective Diode(s)

NOTE: See separate listings for Analog Switch and Analog Multiplexer Substitution Guide and J-FET Replacement Guide.

LEGEND:

PART NO.	Manufacturer's part number, complete for ordering purposes.	
CHAN.	N-Channel, P-Channel or N+P Channel Arrays.	
DESCRP.	DEPL	— Depletion-mode (Normally On.). Unless otherwise stated, all devices are Enhancement-Mode (Normally Off).
	DG	— Dual Gate
	DUAL	— 2-Channel
	OCTAL	— 8-Channel
	QUAD	— 4-Channel
	SOT	— Small Outline Transistor Package.
	Z	— Gate Protective Diode(s).
BV_{DSS}	Drain-Source Breakdown Voltage.	
I_{D(on)}	ON Drain Current at T _C or T _A = +25° C.	
PACKAGE	CHIP	— Individual chips, usually in Waffle Pack.
	CDIP	— Ceramic Dual In-Line on Ceramic Side-Brazed Package.
	LF	— Lead Formed.
	SO-14	— Small Outline, 14-Pin Package.
	TO	— JEDEC Package.
	52+	— 4-Lead variation of TO-52 Package.
	92R	— Reversed Source and Drain Leads.
	143	— SOT-143, Small Outline 4-Pin Package.
TOPAZ PART NUMBER	CF	— Contact Factory for details on available alternative products.
	(Part No.)	— Functional equivalent in similar or identical package which nearly meets, equals, or exceeds key parameters of Part Number.

Ferranti

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
BS107P	N		200	23.000	0.12	92R	SD1122BD
BS107PT	N		200	28.000	0.12	92R	SD1122BD
BS170P	N		60	5.000	0.50	92	BS170
BS250P	P		-60	14.000	-0.23	92	VP0106N3
VN10LP	N		60	5.000	0.27	92	VN10KN3
ZVN0104A	N		40	4.000	0.38	92	SD1107BD
ZVN0104B	N		40	4.000	0.86	205AF	SD1107HD
ZVN0104D	N		40	4.000	0.00	CHIP	SD1107CHP
ZVN0106A	N		60	4.000	0.32	92	SD1107BD
ZVN0106B	N		60	4.000	0.85	205AF	SD1107HD
ZVN0106D	N		60	4.000	0.00	CHIP	SD1107CHP
ZVN0108A	N		80	4.000	0.32	92	SD1107BD
ZVN0108B	N		80	4.000	0.85	205AF	SD1107HD
ZVN0108D	N		80	4.000	0.00	CHIP	SD1107CHP
ZVN0109A	N		90	4.000	0.38	92	SD1107BD
ZVN0109B	N		90	4.000	0.86	205AF	SD1107HD
ZVN0110A	N		100	8.000	0.26	92	SD1107BD
ZVN0110B	N		100	8.000	0.58	205AF	SD1107HD
ZVN0110D	N		100	8.000	0.00	CHIP	SD1107CHP
ZVN0114A	N		140	8.000	0.26	92	SD1112BD
ZVN0114B	N		140	8.000	0.58	205AF	SD1112HD
ZVN0114D	N		140	8.000	0.00	CHIP	SD1112CHP
ZVN0116A	N		160	16.000	0.18	92	SD1112BD
ZVN0116B	N		160	16.000	0.40	205AF	SD1112HD
ZVN0116D	N		160	16.000	0.00	CHIP	SD1112CHP
ZVN0117TA	N		170	23.000	0.16	92	VN2410L
ZVN0120A	N		200	16.000	0.16	92	SD1112BD
ZVN0120B	N		200	16.000	0.42	205AF	SD1112HD
ZVN0120D	N		200	16.000	0.00	CHIP	SD1112CHP
ZVN0124A	N		240	16.000	0.16	92	VN2410L
ZVN0124B	N		240	16.000	0.42	205AF	SD1102HD
ZVN0124D	N		240	16.000	0.00	CHIP	VN2410CHP
ZVN01A2A	N		20	2.000	0.45	92	SD1117BD
ZVN01A2B	N		20	2.000	1.00	205AF	SD1117HD
ZVN01A2D	N		20	2.000	0.00	CHIP	SD1117CHP
ZVN01A3A	N		30	2.000	0.45	92	SD1117BD
ZVN01A3B	N		30	2.000	1.00	205AF	SD1117HD
ZVN01A3D	N		30	2.000	0.00	CHIP	SD1117CHP
ZVN0204B	N		40	2.000	1.32	205AF	SD1117HD
ZVN0204D	N		40	2.000	0.00	CHIP	SD1117CHP
ZVN0206B	N		60	2.000	1.32	205AF	SD1117HD
ZVN0206D	N		60	2.000	0.00	CHIP	SD1117CHP
ZVN0210B	N		100	4.000	0.90	205AF	SD1107HD
ZVN0210D	N		100	4.000	0.00	CHIP	SD1107CHP
ZVN0216B	N		160	8.000	0.64	205AF	SD1112HD
ZVN0216D	N		160	8.000	0.00	CHIP	SD1112CHP
ZVN0220B	N		200	8.000	0.64	205AF	SD1112HD
ZVN0220D	N		200	8.000	0.00	CHIP	SD1112CHP
ZVN02A2B	N		20	1.000	1.80	205AF	SD3301HD
ZVN02A2D	N		20	1.000	0.00	CHIP	SD3301CHP
ZVN02A3B	N		30	1.000	1.80	205AF	SD33301HD
ZVN02A3D	N		30	1.000	0.00	CHIP	SD33301CHP
ZVN0526A	N		260	40.000	0.10	92	SD1101BD
ZVN0530A	N		300	50.000	0.09	92	SD1101BD
ZVN0530B	N		300	50.000	0.15	205AF	SD1101HD

Ferranti (continued)

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
ZVN0530D	N		300	80.000	0.00	CHIP	SD1101CHP
ZVN0535A	N		350	50.000	0.09	92	SD1101BD
ZVN0535B	N		350	50.000	0.15	205AF	SD1101HD
ZVN0535D	N		350	50.000	0.00	CHIP	SD1101CHP
ZVN0540A	N		400	50.000	0.09	92	SD1101BD
ZVN0540B	N		400	50.000	0.15	205AF	SD1101HD
ZVN0540D	N		400	50.000	0.00	CHIP	SD1101CHP
ZVN0545A	N		450	50.000	0.09	92	CF
ZVN0545B	N		450	50.000	0.15	205AF	SD1100HD
ZVN0545D	N		450	50.000	0.00	CHIP	SD1100CHP
ZVN1104B	N		40	1.000	1.90	205AF	SD3301HD
ZVN1104D	N		40	1.000	0.00	CHIP	SD3301CHP
ZVN1106B	N		60	1.000	1.90	205AF	SD3301HD
ZVN1106D	N		60	1.000	0.00	CHIP	SD3301CHP
ZVN1108B	N		80	1.000	1.90	205AF	SD3300HD
ZVN1108D	N		80	1.000	0.00	CHIP	SD3300CHP
ZVN1109B	N		90	1.000	1.90	205AF	SD3300HD
ZVN11A2B	N		20	0.500	2.50	205AF	SD3301HD
ZVN11A2D	N		20	0.500	0.00	CHIP	SD3301CHP
ZVN11A3B	N		30	0.500	2.50	205AF	SD3301HD
ZVN11A3D	N		30	0.500	0.00	CHIP	SD3301CHP
ZVN1204B	N		40	0.400	2.70	205AF	SD3301HD
ZVN1204D	N		40	0.400	0.00	CHIP	SD3301CHP
ZVN1206B	N		60	0.400	2.70	205AF	SD3301HD
ZVN1206D	N		60	0.400	0.00	CHIP	SD3301CHP
ZVN1210B	N		100	0.750	2.00	205AF	SD3300HD
ZVN1210D	N		100	0.750	0.00	CHIP	SD3300CHP
ZVN1304A	N		40	10.000	0.23	92	SD1107BD
ZVN1304B	N		40	10.000	0.52	205AF	SD1107HD
ZVN1304D	N		40	10.000	0.00	CHIP	SD1107CHP
ZVN1306A	N		60	10.000	0.20	92	SD1107BD
ZVN1306B	N		60	10.000	0.50	205AF	SD1107HD
ZVN1306D	N		60	10.000	0.00	CHIP	SD1107CHP
ZVN1308A	N		80	10.000	0.20	92	SD1107BD
ZVN1308B	N		80	10.000	0.50	205AF	SD1107HD
ZVN1308D	N		80	10.000	0.00	CHIP	SD1107CHP
ZVN1309A	N		90	10.000	0.23	92	SD1107BD
ZVN1309B	N		90	10.000	0.52	205AF	SD1107HD
ZVN1310A	N		100	20.000	0.16	92	SD1107BD
ZVN1310B	N		100	20.000	0.37	205AF	SD1107HD
ZVN1310D	N		100	20.000	0.00	CHIP	SD1107CHP
ZVN1314A	N		140	20.000	0.16	92	SD1113BD
ZVN1314B	N		140	20.000	0.37	205AF	SD1113HD
ZVN1314D	N		140	20.000	0.00	CHIP	SD1113CHP
ZVN1316A	N		160	40.000	0.12	92	SD1113BD
ZVN1316B	N		160	40.000	0.26	205AF	SD1113HD
ZVN1316D	N		160	40.000	0.00	CHIP	SD1113CHP
ZVN1320A	N		200	40.000	0.10	92	SD1113BD
ZVN1320B	N		200	40.000	0.25	205AF	SD1113HD
ZVN1320D	N		200	40.000	0.00	CHIP	SD1113CHP
ZVN1404A	N		40	250.000	0.01	92	SD1202BD
ZVN1404D	N		40	250.000	0.00	CHIP	SD1202CHP
ZVN1406A	N		60	250.000	0.01	92	SD1202BD
ZVN1406D	N		60	250.000	0.00	CHIP	SD1202CHP
ZVN1408A	N		80	250.000	0.01	92	SD1202BD

Ferranti (continued)

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
ZVN1408D	N		80	250.000	0.00	CHIP	SD1202CHP
ZVN1409A	N		90	250.000	0.01	92	SD1202BD
ZVN1409D	N		90	250.000	0.00	CHIP	SD1202CHP
ZVN1410A	N		100	500.000	0.03	92	SD1202BD
ZVN1410D	N		100	500.000	0.00	CHIP	SD1202CHP
ZVN1414A	N		140	500.000	0.03	92	SD1202BD
ZVN1414D	N		140	500.000	0.00	CHIP	SD1202CHP
ZVN1416A	N		160	1000.000	0.02	92	SD1202BD
ZVN1416D	N		160	1000.000	0.00	CHIP	SD1202CHP
ZVN1420A	N		200	1000.000	0.02	92	SD1202BD
ZVN1420D	N		200	1000.000	0.00	CHIP	SD1202CHP
ZVN2104A	N		40	2.000	0.45	92	CF
ZVN2104B	N		40	2.000	1.20	205AF	CF
ZVN2106A	N		60	2.000	0.45	92	CF
ZVN2106B	N		60	2.000	1.20	205AF	CF
ZVN2106D	N		60	2.000	0.00	CHIP	CF
ZVN2110A	N		100	4.000	0.32	92	SD1107BD
ZVN2110B	N		100	4.000	0.85	205AF	SD1107HD
ZVN2110D	N		100	4.000	0.00	CHIP	SD1107CHP
ZVN2115A	N		150	16.000	0.16	92	SD1113BD
ZVN2115B	N		150	16.000	0.42	205AF	SD1113HD
ZVN2117A	N		170	10.000	0.17	92	SD1113BD
ZVN2117B	N		170	10.000	0.46	205AF	SD1113HD
ZVN2120A	N		200	10.000	0.18	92	SD1113BD
ZVN2120B	N		200	10.000	0.46	205AF	SD1113HD
ZVN2120D	N		200	10.000	0.00	CHIP	SD1113CHP
ZVN2202B	N		20	0.500	4.80	205AF	SD3301HD
ZVN2204B	N		40	0.500	4.80	205AF	SD3301HD
ZVN2206B	N		60	0.500	4.80	205AF	SD3301HD
ZVN2206D	N		60	0.500	0.00	CHIP	SD3301CHP
ZVN2208B	N		80	0.800	3.45	205AF	SD3300HD
ZVN2210B	N		100	0.800	3.45	205AF	SD3300HD
ZVN2210D	N		100	0.800	0.00	CHIP	SD3300CHP
ZVN2530A	N		300	35.000	0.09	92	SD1101BD
ZVN2530B	N		300	35.000	0.24	205AF	SD1101HD
ZVN2535A	N		350	35.000	0.09	92	SD1101BD
ZVN2535B	N		350	35.000	0.25	205AF	SD1101HD
ZVN2535D	N		350	35.000	0.00	CHIP	SD1101CHP
ZVN3302A	N		20	5.000	0.27	92	VN0104N3
ZVN3302B	N		20	5.000	0.75	205AF	SD1117HD
ZVN3304A	N		40	5.000	0.27	92	VN0104N3
ZVN3304B	N		40	5.000	0.75	205AF	SD1117HD
ZVN3306A	N		60	5.000	0.27	92	VN0106N3
ZVN3306B	N		60	5.000	0.75	205AF	SD1117HD
ZVN3306D	N		60	5.000	0.00	CHIP	SD1107CHP
ZVN3310A	N		100	10.000	0.20	92	SD1107BD
ZVN3310B	N		100	10.000	0.50	205AF	SD1107HD
ZVN3310D	N		100	10.000	0.00	CHIP	SD1107CHP
ZVN3315A	N		150	40.000	0.10	92	SD1113BD
ZVN3315B	N		150	40.000	0.25	205AF	SD1113HD
ZVN3320A	N		200	25.000	0.10	92	SD1113BD
ZVN3320B	N		200	25.000	0.25	205AF	SD1113HD
ZVN3320D	N		200	25.000	0.00	CHIP	SD1113CHP
ZVN4206A	N		60	1.000	0.60	92	SD3301BD
ZVNL 120A	N		200	10.000	0.18	92	VN2410L

Ferranti (continued)

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
ZVNL535A	N		350	40.000	0.09	92	SD1101BD
ZVP0102A	P		-20	5.000	-0.28	92	SD2107BD
ZVP0102B	P		-20	5.000	-0.76	205AF	SD2107HD
ZVP0104A	P		-40	8.000	-0.27	92	VP0104N3
ZVP0104B	P		-40	8.000	-0.62	205AF	SD2107HD
ZVP0104D	P		-40	8.000	0.00	CHIP	VP0104ND
ZVP0106A	P		-60	8.000	-0.23	92	VP0106N3
ZVP0106B	P		-60	8.000	-0.60	205AF	SD2107HD
ZVP0106D	P		-60	8.000	0.00	CHIP	VP0106ND
ZVP0108A	P		-80	8.000	-0.23	92	VP0109N3
ZVP0108B	P		-80	8.000	-0.60	205AF	SD2107HD
ZVP0108D	P		-80	8.000	0.00	CHIP	VP0109ND
ZVP0109A	P		-90	8.000	-0.27	92	VP0109N3
ZVP0109B	P		-90	8.000	-0.62	205AF	SD2107HD
ZVP0110A	P		-100	16.000	-0.20	92	SD2107BD
ZVP0110B	P		-100	16.000	-0.44	205AF	SD2107HD
ZVP0110D	P		-100	16.000	0.00	CHIP	SD2107CHP
ZVP0204B	P		-40	4.000	-1.00	205AF	SD2107HD
ZVP0204D	P		-40	4.000	0.00	CHIP	SD2107CHP
ZVP0206B	P		-60	4.000	-1.00	205AF	SD2107HD
ZVP0206D	P		-60	4.000	0.00	CHIP	SD2107CHP
ZVP0208B	P		-80	4.000	-1.00	205AF	SD2107HD
ZVP0208D	P		-80	4.000	0.00	CHIP	SD2107CHP
ZVP0209B	P		-90	4.000	-1.00	205AF	SD2107HD
ZVP0210B	P		-100	8.000	-0.64	205AF	SD2107HD
ZVP0210D	P		-100	8.000	0.00	CHIP	SD2107CHP
ZVP1110B	P		-100	4.000	-0.97	205AF	SD2107HD
ZVP1110D	P		-100	4.000	0.00	CHIP	SD2107CHP
ZVP1404A	P		-40	600.000	-0.03	92	SD2204BD
ZVP1406A	P		-60	600.000	-0.03	92	SD2204BD
ZVP1408A	P		-80	600.000	-0.03	92	SD2204BD
ZVP1409A	P		-90	600.000	-0.03	92	SD2204BD
ZVP1410A	P		-100	1200.000	-0.02	92	SD2204BD
ZVP1414A	P		-140	1200.000	-0.02	92	SD2204BD
ZVP1416A	P		-160	2400.000	-0.02	92	SD2204BD
ZVP1420A	P		-200	2400.000	-0.02	92	SD2204BD
ZVP2104A	P		-40	5.000	-0.28	92	SD2107BD
ZVP2104B	P		-40	5.000	-0.76	205AF	SD2107HD
ZVP2106A	P		-60	5.000	-0.28	92	SD2107BD
ZVP2106B	P		-60	5.000	-0.76	205AF	SD2107HD
ZVP2106D	P		-60	5.000	0.00	CHIP	SD2107CHP
ZVP2110A	P		-100	8.000	-0.23	92	SD2107BD
ZVP2110B	P		-100	8.000	-0.60	205AF	SD2107HD
ZVP2110D	P		-100	8.000	0.00	CHIP	SD2107CHP
ZVP3302A	P		-20	14.000	-0.16	92	VP0104N3
ZVP3304A	P		-40	14.000	-0.16	92	VP0104N3
ZVP3306A	P		-60	14.000	-0.16	92	VP0106N3
ZVP3306B	P		-60	14.000	-0.40	205AF	SD2107HD
ZVP3306D	P		-60	14.000	0.00	CHIP	SD2107CHP
ZVP3310A	P		-100	20.000	-0.14	92	SD2107BD
ZVP3310B	P		-100	20.000	-0.30	205AF	SD2107HD
ZVP3310D	P		-100	20.000	0.00	CHIP	SD2107CHP

General Electric/Intersil

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
D80AK2	N		60	2.400	0.50	237	CF
IRFF110	N		100	0.600	3.50	205AF	SD3300HD
IRFF111	N		60	0.600	3.50	205AF	SD3301HD
IRFF112	N		100	0.800	3.00	205AF	SD3300HD
IRFF113	N		60	0.800	3.00	205AF	SD3301HD
IRFF123	N		60	0.400	5.00	205AF	SD3301HD
IVN5000AND	N		40	2.500	0.70	237	CF
IVN5000ANE	N		60	2.500	0.70	237	CF
IVN5000ANF	N		80	2.500	0.70	237	CF
IVN5000ANH	N		100	2.500	0.70	237	CF
IVN5000SND	N		40	2.500	0.90	52	SD1117DD
IVN5000SNE	N		60	2.500	0.90	52	SD1117DD
IVN5000TND	N		40	2.500	1.20	205AF	SD1117HD
IVN5000TNE	N		60	2.500	1.20	205AF	SD1117HD
IVN5000TNF	N		80	2.500	1.20	205AF	CF
IVN5000TNG	N		90	2.500	1.20	205AF	CF
IVN5000TNH	N		100	2.500	1.20	205AF	CF
IVN5001AND	N		40	2.500	0.70	237	CF
IVN5001ANE	N		60	2.500	0.70	237	CF
IVN5001ANF	N		80	2.500	0.70	237	CF
IVN5001ANH	N		100	2.500	0.70	237	CF
IVN5001SND	N		40	2.500	0.90	52	SD1117DD
IVN5001SNE	N		60	2.500	0.90	52	SD1117DD
IVN5001TND	N		40	2.500	1.20	205AF	SD1117HD
IVN5001TNE	N		60	2.500	1.20	205AF	SD1117HD
IVN5001TNF	N		80	2.500	1.20	205AF	SD1117HD
IVN5001TNG	N		90	2.500	1.20	205AF	SD1107HD
IVN5200TND	N		40	0.500	4.00	205AF	SD3301HD
IVN5200TNE	N		60	0.500	4.00	205AF	SD3301HD
IVN5200TNF	N		80	0.500	4.00	205AF	SD3300HD
INV5201TND	N		40	0.500	4.00	205AF	SD3301HD
INV5201TNE	N		60	0.500	4.00	205AF	SD3301HD
INV5201TNF	N		80	0.500	4.00	205AF	SD3300HD
INV6300ANE	N		60	7.500	0.25	237	SD1106AD
INV6300ANF	N		80	7.500	0.25	237	SD1106AD
INV6300SNE	N		60	7.500	0.25	52	SD1107DD
INV6300SNF	N		80	7.500	0.25	52	SD1107DD
INV6300SNH	N		100	7.500	0.25	52	SD1107DD
INV6300SNM	N		200	25.000	0.12	52	SD1113DD
INV6300SNP	N		250	25.000	0.12	52	SD1102DD
INV6300SNS	N		400	75.000	0.10	52	SD1101DD
INV6300SNT	N		450	75.000	0.10	52	SD1100DD
IVN6660	N	Z	60	3.000	2.40	205AF	SD1117HD
IVN6661	N	Z	90	4.000	2.40	205AF	SD1107HD
VN10KMA	N		60	5.000	0.75	237	SD1106AD

General Electric/RCA

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
2N6782	N		100	0.600	3.50	205AF	2N6782
IRFF110	N		100	0.600	3.50	205AF	SD3300HD
IRFF111	N		60	0.600	3.50	205AF	SD3301HD
IRFF112	N		100	0.800	3.00	205AF	SD3300HD
IRFF113	N		60	0.800	3.00	250AF	SD3301HD

General Electric/RCA (continued)

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
IRFF123	N		60	0.400	5.00	205AF	SD3301HD
RFL1N08L	N		80	1.200	1.00	205AF	SD3300HD
RFL1N10L	N		100	1.200	1.00	205AF	SD3300HD
RFL2N05	N		50	0.750	2.00	205AF	SD3301HD
RFL2N06	N		60	0.750	2.00	205AF	SD3301HD

Hitachi

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
2SK196H	N	Z	160	15.000	0.50	205AF	SD1113HD
2SK441	N		500	50.000	0.30	205AF	CF

International Rectifier

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
2N6782	N		100	0.600	3.50	205AF	2N6782
IRFC110	N		100	0.600	0.00	CHIP	SD3300CHP
IRFC113	N		60	0.800	0.00	CHIP	SD3301CHP
IRFC123	N		60	0.400	0.00	CHIP	SD3301CHP
IRFC1Z0	N		100	2.400	0.00	CHIP	CF
IRFC1Z3	N		60	3.200	0.00	CHIP	SD1117CHP
IRFF110	N		100	0.600	3.50	205AF	SD3300HD
IRFF111	N		60	0.600	3.50	205AF	SD3301HD
IRFF112	N		100	0.800	3.00	205AF	SD3300HD
IRFF113	N		60	0.800	3.00	205AF	SD3301HD
IRFF123	N		60	0.400	5.00	205AF	SD3301HD
IRFG1Z0	N	QUAD	100	2.600	0.45	14SDIP	CF
IRFG1Z3	N	QUAD	60	3.400	0.38	14SDIP	CF
IRFS1Z3	N	SMD	60	3.200	0.75	SOT-89	CF

ITT Semiconductor

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
BS107	N		200	28.000	0.08	92LF	SD1122BD
BS170	N		60	5.000	0.19	92R	BS170
BS250	P		-45	14.000	-0.13	92LF	VP0106N3

Motorola

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
2N6659	N		35	1.800	1.00	205AD	CF
2N6660	N		60	3.000	2.00	205AF	SD1117HD
2N6661	N		90	4.000	2.00	205AF	SD1107HD
2N7000	N		60	5.000	0.20	226AA	2N7000
2N7007	N		240	45.000	0.15	226AA	VN2410L

Motorola (continued)

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
2N7008	N		60	7.500	0.30	226AA	CF
BS107	N		200	28.000	0.25	226AA	SD1122BD
BS107A	N		200	6.000	0.25	226AA	CF
BS108	N		200	8.500	0.20	226AA	SD1112BD
BS170	N		60	5.000	0.50	226AA	BS170
BS170P	P		-60	5.000	-0.50	226AA	VP0808L
BS250	P		-45	14.000	-0.13	226AA	VP0106N3
MFE350	N		350	35.000	0.20	205AD	SD1101HD
MFE500	N		500	50.000	0.20	205AD	CF
MFE910	N		60	5.000	0.50	205AF	SD1117HD
MFE9200	N		200	6.400	0.40	206	SD1112DD
MFE930	N		35	1.400	2.00	205AF	SD3301HD
MFE960	N		60	1.700	2.00	205AF	SD3301HD
MFE990	N		90	2.000	2.00	205AF	SD3300HD
MFQ1000C	N	QUAD	60	10.000	0.00	14CDIP	CF
MFQ107P	N	QUAD	200	14.000	0.00	14PDIP	CF
MFQ170P	N	QUAD	50	5.000	0.00	14PDIP	SD1117N
MFQ6660C	N	QUAD	60	3.000	0.00	14CDIP	CF
MFQ6660P	N	QUAD	35	3.000	0.00	14PDIP	SD1117N
MFQ6661P	N	QUAD	90	4.000	0.00	14PDIP	SD1107N
MPF350	N	DEPL	350	35.000	0.15	226AA	SD1101BD
MPF480	N		80	80.000	0.10	226AA	CF
MPF481	N		180	140.000	0.10	226AA	CF
MPF500	N		500	50.000	0.10	226AA	SD1500BD
MPF6659	N		35	1.800	0.50	226AE	CF
MPF6660	N		60	3.000	0.30	226AE	SD1117BD
MPF6661	N		90	4.000	0.25	226AE	SD1107BD
MPF910	N		60	5.000	0.20	226AE	SD1107BD
MPF9200	N		200	6.400	0.40	226	SD1112BD
MPF930	N		35	1.400	2.00	226AE	SD3301BD
MPF960	N		60	1.700	2.00	226AE	SD3301BD
MPF990	N		90	2.000	2.00	226AE	SD3300BD
MXF500	N		500	50.000	0.10	SOT-89	SD1500CY
VN0300B	N		30	1.200	1.00	205AD	SD3301HD
VN0300L	N		30	1.200	0.63	226AA	SD3301BD
VN0610LL	N		60	5.000	0.19	226AA	VN0610LL
VN1706B	N		170	6.000	0.63	205AD	CF
VN1706L	N		170	6.000	0.16	226AA	CF
VN1710B	N		170	10.000	0.60	205AD	CF
VN1710L	N		170	10.000	0.12	226AA	VN2410L
VN2222LL	N		60	7.500	0.30	226AA	VN2222LL
VN2406B	N		240	6.000	0.63	205AD	CF
VN2406L	N		240	6.000	0.16	226AA	CF
VN2410B	N		240	10.000	0.60	205AD	CF
VN2410L	N		240	10.000	0.12	226AA	VN2410L

NEC

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
2SK679	N		30	0.500	0.50	92	SD3301BD

Philips/Amperex/Mullard/RTC/Valvo

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
2N6659	N		35	1.800	1.40	205AF	CF
2N6660	N		60	3.000	1.10	205AF	SD1117HD
BS170	N		60	5.000	0.19	92LF	BS170
BSD212	N		10	70.000	0.05	72	SD212DE
BSD213	N	Z	10	70.000	0.05	72	SD213DE
BSD214	N		20	70.000	0.05	72	SD214DE
BSD215	N	Z	20	70.000	0.05	72	SD215DE
BST70A	N		80	4.000	0.50	92	SD1107BD
BST72A	N		100	10.000	0.30	92	SD1107BD
BST90	N		80	4.000	0.50	205AF	SD1107HD
SD5000N	N	Z QUAD	20	70.000	0.05	16PDIP	SD5000N
SD5001N	N	Z QUAD	10	70.000	0.05	16PDIP	SD5001N
SD5002N	N	Z QUAD	15	70.000	0.05	16PDIP	SD5002N
SD5100N	N	Z QUAD	30	70.000	0.05	14PDIP	SD5100N
SD5200N	N	Z QUAD	30	80.000	0.05	16PDIP	SD5200N
SD5400CY	N	Z QUAD	20	70.000	0.05	SO-14	SD5400CY
SD5401CY	N	Z QUAD	10	70.000	0.05	SO-14	SD5401CY
SD5402CY	N	Z QUAD	15	70.000	0.05	SO-14	SD5402CY

Signetics

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
DMP4025DB	N		25	6.000	0.80	205AF	SD205HD
DMS4025DE	N		25	6.000	0.20	72	SD217DE
SD200DC	N		25	50.000	0.05	52+	SD200DC
SD201DC	N	Z	25	50.000	0.05	52+	SD201DC
SD202DC	N		20	35.000	0.05	52+	SD202DC
SD203DC	N	Z	20	35.000	0.05	52+	SD203DC
SD210DE	N		30	70.000	0.05	72	SD210DE
SD210EE	N		30	70.000	0.05	72	SD210DE
SD211DE	N	Z	30	70.000	0.05	72	SD211DE
SD211EE	N	Z	30	70.000	0.05	72	SD211DE
SD212DE	N		10	70.000	0.05	72	SD212DE
SD212EE	N		10	70.000	0.05	72	SD212DE
SD213DE	N	Z	10	70.000	0.05	72	SD213DE
SD213EE	N	Z	10	70.000	0.05	72	SD213DE
SD214DE	N		20	70.000	0.05	72	SD214DE
SD215DE	N	Z	20	70.000	0.05	72	SD215DE
SD215EE	N	Z	20	70.000	0.05	72	SD215DE
SD217DE	N	Z	25	6.000	0.30	72	SD217DE
SD217EE	N	Z	25	6.000	0.30	72	SD217DE
SD220H	N		60	9.000	0.50	205AF	SD220HD
SD222DC	N		60	9.000	0.50	72	CF
SD300DC	N	Z DG	25	130.000	0.05	52+	SD304DE
SD300EC	N	Z DG	25	130.000	0.05	52+	SD304DE
SD303DC	N	Z DG	20	80.000	0.05	52+	SD303DC
SD303EC	N	Z DG	20	80.000	0.05	52+	SD303DC
SD304DE	N	Z DG	25	130.000	0.05	72	SD304DE
SD304EE	N	Z DG	25	130.000	0.05	72	SD304DE
SD306DE	N	Z DG	20	100.000	0.05	72	SD306DE
SD306EE	N	Z DG	20	100.000	0.05	72	SD306DE
SD5000J	N	Z QUAD	20	70.000	0.05	16CDIP	SD5000J
SD5000N	N	Z QUAD	20	70.000	0.05	16PDIP	SD5000N
SD5001J	N	Z QUAD	10	70.000	0.05	16CDIP	SD5001J
SD5001N	N	Z QUAD	10	70.000	0.05	16PDIP	SD5001N
SD5002J	N	Z QUAD	15	70.000	0.05	16CDIP	SD5002J
SD5002N	N	Z QUAD	15	70.000	0.05	16PDIP	SD5002N

Signetics (continued)

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
SD5100N	N	Z QUAD	30	70.000	0.05	14PDIP	SD5100N
SD5101N	N	Z QUAD	15	70.000	0.05	14PDIP	SD5101N
SD5200I	N	Z QUAD	30	80.000	0.05	16CDIP	CF
SD5200N	N	Z QUAD	30	80.000	0.05	16PDIP	SD5200N

Siliconix

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
2N6659	N		35	1.800	1.40	205AF	CF
2N6660	N		60	3.000	2.00	205AF	SD1117HD
2N6661	N		90	4.000	2.00	205AF	SD1107HD
2N6781	N		60	0.600	3.50	205AF	2N6781
2N6782	N		100	0.600	3.50	205AF	2N6782
2N7000	N		60	5.000	0.20	92	2N7000
2N7008	N		60	7.500	0.25	92	CF
2N7010	N		60	0.350	1.30	237	CF
2N7011	N		40	0.350	1.30	237	CF
2N7104	N	(210)	30	70.000	0.05	72	2N7104
2N7105	N	Z(211)	30	70.000	0.05	72	2N7105
2N7106	N	(212)	10	70.000	0.05	72	2N7106
2N7107	N	Z(213)	10	70.000	0.05	72	2N7107
2N7108	N	(214)	10	70.000	0.05	72	2N7108
2N7109	N	Z(215)	10	70.000	0.05	72	2N7109
2N7116	N	Z QUAD	20	70.000	0.05	16SDIP	CF
2N7117	N	Z QUAD	10	70.000	0.05	16SDIP	CF
2N7118	N	Z QUAD	15	70.000	0.05	16SDIP	CF
BS107	N		200	28.000	0.08	92LF	SD1122BD
BS170	N		60	5.000	0.19	92LF	BS170
BS250	P		-45	14.000	-0.13	92LF	VP0106N3
BSR64	N		60	7.500	0.25	237	SD1106AD
BSR65	N		60	5.000	0.30	237	SD1106AD
BSR66	N		60	3.000	0.47	237	SD1106AD
BSR67	N		80	4.000	0.40	237	SD1106AD
IRFF110	N		100	0.600	3.50	205AF	SD3300HD
IRFF111	N		60	0.600	3.50	205AF	SD3301HD
IRFF112	N		100	0.800	3.00	205AF	SD3300HD
IRFF113	N		60	0.800	3.00	205AF	SD3301HD
IRFF123	N		60	0.400	5.00	205AF	SD3301HD
SD2100	N	DEPL	25	200.000	0.05	72	SD2100DE
SD210DE	N		30	70.000	0.05	72	SD210DE/R
SD2110	N	DUAL	25	60.000	0.05	78	SD411HD
SD211DE	N	Z	30	70.000	0.05	72	SD211DE/R
SD2120	N	DUAL	25	60.000	0.05	78	SD411HD
SD212DE	N		10	70.000	0.05	72	SD212DE/R
SD213DE	N	Z	10	70.000	0.05	72	SD213DE/R
SD214DE	N		20	70.000	0.05	72	SD214DE/R
SD215DE	N	Z	20	70.000	0.05	72	SD215DE/R
SD5000I	N	Z QUAD	20	70.000	0.05	16CDIP	SD5000J
SD5000N	N	Z QUAD	20	70.000	0.05	16PDIP	SD5000N
SD5001I	N	Z QUAD	10	70.000	0.05	16CDIP	SD5001J
SD5001N	N	Z QUAD	10	70.000	0.05	16PDIP	SD5001N
SD5002I	N	Z QUAD	15	70.000	0.05	16CDIP	SD5002J
SD5002N	N	Z QUAD	15	70.000	0.05	16PDIP	SD5002N

Siliconix (continued)

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
SD5200I	N	Z QUAD	30	80.000	0.05	16CDIP	CF
SD5200N	N	Z QUAD	30	80.000	0.05	16PDIP	SD5200N
SD5400CY	N	Z QUAD	20	70.000	0.05	SO-14	SD5400CY
SD5401CY	N	Z QUAD	10	70.000	0.05	SO-14	SD5401CY
SD5402CY	N	Z QUAD	15	70.000	0.05	SO-14	SD5402CY
SI2200	N		15	16.000	0.00	72	SD217DE
SI2400	N	Z	15	12.000	0.05	72	SD217DE
SN0120NA	N	OCTAL	200	350.000	0.03	18PDIP	AN0120NA
SN0120NB	N	OCTAL	200	300.000	0.05	18CDIP	AN0120NA
SN0130NA	N	OCTAL	300	350.000	0.03	18PDIP	AN0130NA
SN0130NB	N	OCTAL	300	300.000	0.05	18CDIP	AN0130NA
SN0140NA	N	OCTAL	400	400.000	0.02	18PDIP	AN0140NA
SN0140NB	N	OCTAL	400	350.000	0.05	18CDIP	AN0140NA
SST211	N	Z	30	75.000	0.05	SOT143	SST211
SST213	N	Z	10	75.000	0.05	SOT143	SST213
SST215	N	Z	20	75.000	0.05	SOT143	SST215
VN0300B	N		30	1.200	1.86	205AF	SD3301HD
VN0300L	N		30	1.200	0.63	92	SD3301BD
VN0300M	N		30	1.200	0.75	237	SD3301AD
VN0606M	N		60	3.000	0.47	237	SD1106AD
VN0610L	N	Z	60	5.000	0.19	92	SD1117BD
VN0610LL	N		60	5.000	0.19	92	VN0610LL
VN0808M	N		80	4.000	0.40	237	CF
VN1008L	N		120	5.000	0.23	92	CF
VN10KE	N	Z	60	5.000	0.17	52	SD1107DD
VN10KM	N	Z	60	5.000	0.30	237	SD1106AD
VN10LE	N		60	5.000	0.17	52	SD1106DD
VN10LM	N		60	5.000	0.30	237	VN10LM
VN1206B	N		120	6.000	0.63	205AF	CF
VN1206L	N		120	6.000	0.16	92	CF
VN1206M	N		120	6.000	0.25	237	CF
VN1210L	N		120	10.000	0.12	92	VN2410L
VN1210M	N		120	10.000	0.19	237	CF
VN1706B	N		170	6.000	0.63	205AF	CF
VN1706L	N		170	6.000	0.16	92	CF
VN1706M	N		170	6.000	0.25	237	CF
VN1710L	N		170	10.000	0.12	92	VN2410L
VN1710M	N		170	10.000	0.19	237	CF
VN1720M	N		170	20.000	0.14	237	CF
VN2010L	N		200	10.000	0.25	92	VN2410L
VN2020L	N		200	24.000	0.08	92	CF
VN2222KM	N	Z	60	7.500	0.25	237	SD1106AD
VN2222L	N	Z	60	7.500	0.15	92	SD1117BD
VN2222LL	N		60	7.500	0.15	92	VN2222LL
VN2222LM	N		60	7.500	0.25	237	VN2222LM
VN2406B	N		240	6.000	0.63	205AF	CF
VN2406L	N		240	6.000	0.16	92	CF
VN2406M	N		240	6.000	0.25	237	CF
VN2410L	N		240	10.000	0.12	92	VN2410L
VN2410M	N		240	10.000	0.19	237	VN2410M
VN2420L	N		240	24.000	0.08	92	CF
VN3515L	N		350	15.000	0.00	92	CF
VN35AB	N		35	2.500	1.29	205AF	SD1117HD
VN4012L	N		400	12.000	0.00	92	CF
VN6035L	N		600	35.000	0.00	92	SD1500BD

Siliconix (continued)

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
VN67AB	N		60	3.500	1.09	205AF	SD1117HD
VP0610L	P		-60	10.000	0.40	92	VP0106N3
VN90AB	N		90	5.000	0.91	205AF	SD1107HD
VN99AB	N		90	4.500	0.96	205AF	SD1107HD
VNC010B	N		60	0.500	4.00	205AF	SD3301HD
VNC011B	N		60	0.500	4.00	205AF	SD3301HD
VND010B	N		80	0.500	4.00	205AF	SD3300HD
VND011B	N		80	0.500	4.00	205AF	SD3300HD
VNE010B	N		100	0.500	4.00	205AF	SD3300HD
VNE011B	N		100	0.500	4.00	205AF	SD3300HD
VP0614L	P		-60	14.000	-0.40	92	VP0106N3
VP0808B	P		-80	5.000	-0.88	205AF	SD2107HD
VP0808L	P		-80	5.000	-0.21	92	VP0808L
VP0808M	P		-80	5.000	-0.33	237	VP0808M
VP1008B	P		-100	5.000	-0.88	205AF	SD2107HD
VP1008L	P		-100	5.000	-0.21	92	VP1008L
VP1008M	P		-100	5.000	-0.33	237	VP1008M
VQ1000J	N	QUAD	60	5.500	0.22	14PDIP	VQ1000J
VQ1004J	N	QUAD	60	3.500	0.46	14PDIP	SD1117N
VQ1006J	N	QUAD	60	4.500	0.40	14PDIP	SD1107N
VQ2004J	P	QUAD	-60	5.000	-0.41	14PDIP	CF
VQ2006J	P	QUAD	-90	5.000	-0.41	14PDIP	CF

Semi Processes, Inc.

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
SD1100CHP	N		450	35.000	0.00	CHIP	SD1100CHP
SD1100DD	N		450	35.000	0.08	18	SD1100DD
SD1100HD	N		450	35.000	0.08	205AF	SD1100HD
SD1101BD	N		400	25.000	0.08	92	SD1101BD
SD1101CHP	N		400	25.000	0.00	CHIP	SD1101CHP
SD1101DD	N		400	25.000	0.08	18	SD1101DD
SD1101HD	N		400	25.000	0.14	205AF	SD1101HD
SD1102BD	N		250	10.000	0.23	92	SD1102BD
SD1102CHP	N		250	10.000	0.00	CHIP	SD1102CHP
SD1102DD	N		250	10.000	0.31	18	SD1102DD
SD1102HD	N		250	10.000	0.57	205AF	SD1102HD
SD1104BD	N		100	3.000	0.42	92	SD1107BD
SD1104CHP	N		100	3.000	0.00	CHIP	SD1107CHP
SD1104DD	N		100	3.000	0.56	18	SD1107DD
SD1104HD	N		100	3.000	1.05	205AF	SD1107HD
SD1105BD	N		100	4.000	0.36	92	SD1107BD
SD1105CHP	N		100	4.000	0.00	CHIP	SD1107CHP
SD1105DD	N		100	4.000	0.49	18	SD1107DD
SD1105HD	N		100	4.000	0.91	205AF	SD1107HD
SD1106AD	N		60	5.000	0.50	237	SD1106AD
SD1106CHP	N		60	5.000	0.00	CHIP	SD1106CHP
SD1106DD	N		60	5.000	0.50	18	SD1106DD
SD1107BD	N		100	4.000	0.36	92	SD1107BD
SD1107CHP	N		100	4.000	0.00	CHIP	SD1107CHP
SD1107DD	N		100	4.000	0.49	18	SD1107DD
SD1107HD	N		100	4.000	0.91	205AF	SD1107HD
SD1107N	N	QUAD	100	4.000	0.51	14PDIP	SD1107N
SD1112BD	N		200	7.000	0.27	92	SD1112BD
SD1112CHP	N		200	7.000	0.00	CHIP	SD1112CHP
SD1112DD	N		200	7.000	0.37	18	SD1112DD

Semi Processes, Inc. (continued)

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
SD1112HD	N		200	7.000	0.69	205AF	SD1112HD
SD1113BD	N		200	10.000	0.23	92	SD1113BD
SD1113CHP	N		200	10.000	0.00	CHIP	SD1113CHP
SD1113DD	N		200	10.000	0.31	18	SD1113DD
SD1113HD	N		200	10.000	0.57	205AF	SD1113HD
SD1114BD	N		80	3.000	0.42	92	SD1107BD
SD1114CHP	N		80	3.000	0.00	CHIP	SD1107CHP
SD1114DD	N		80	3.000	0.56	18	SD1107DD
SD1114HD	N		80	3.000	1.05	205AF	SD1107HD
SD1115BD	N		80	4.000	0.42	92	SD1107BD
SD1115CHP	N		80	4.000	0.00	CHIP	SD1107CHP
SD1115DD	N		80	4.000	0.49	18	SD1107DD
SD1115HD	N		80	4.000	0.91	205AF	SD1107HD
SD1117BD	N		60	2.500	0.46	92	SD1117BD
SD1117CHP	N		60	2.500	0.00	CHIP	SD1117CHP
SD1117DD	N		60	2.500	0.62	18	SD1117DD
SD1117HD	N		60	2.500	1.15	205AF	SD1117HD
SD1117N	N	QUAD	60	2.500	0.46	14PDIP	SD1117N
SD1122BD	N		200	10.000	0.12	92LF	SD1122BD
SD1122CHP	N		200	10.000	0.00	CHIP	SD1122CHP
SD1124BD	N		60	5.000	0.20	92R	BS170
SD1124CHP	N		60	5.000	0.00	CHIP	SD1124CHP
SD1200CHP	N		450	700.000	0.00	CHIP	SD1200CHP
SD1200DD	N		450	700.000	0.02	18	SD1200DD
SD1201CHP	N		400	500.000	0.00	CHIP	SD1201CHP
SD1201DD	N		400	500.000	0.02	18	SD1201DD
SD1202BD	N		200	250.000	0.04	92	SD1202BD
SD1202CHP	N		200	250.000	0.00	CHIP	SD1202CHP
SD200DC/R	N		25	50.000	0.05	52+	SD200DC/R
SD201DC/R	N	Z	25	50.000	0.05	52+	SD201DC/R
SD202DC/R	N		20	35.000	0.05	52+	SD202DC/R
SD203DC/R	N	Z	20	35.000	0.05	52+	SD203DC/R
SD210DE/R	N		30	70.000	0.05	72	SD210DE/R
SD211DE/R	N	Z	30	70.000	0.05	72	SD211DE/R
SD212DE/R	N		10	70.000	0.05	72	SD212DE/R
SD213DE/R	N	Z	10	70.000	0.05	72	SD213DE/R
SD214DE/R	N		20	70.000	0.05	72	SD214DE/R
SD214EE	N		20	70.000	0.05	72	SD214DE
SD215DE/R	N	Z	20	70.000	0.05	72	SD215DE/R
SD303DC/R	N	Z DG	20	80.000	0.05	52+	SD303DC/R
SD304DE/R	N	Z DG	25	130.000	0.05	72	SD304DE/R
SD306DE/R	N	Z DG	20	100.000	0.05	72	SD306DE/R

Supertex

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
2N6659	N		35	1.800	1.40	205AF	CF
2N6660	N		60	3.000	2.00	205AF	SD1117HD
2N6661	N		90	4.000	2.00	205AF	SD1107HD
2N7000	N		60	5.000	0.20	92	2N7000
2N7007	N		240	45.000	0.15	92	VN2410L
2N7008	N		60	7.500	0.30	92	CF
AN0116NA	N	OCTAL	160	350.000	0.03	18PDIP	AN0120NA
AN0116NB	N	OCTAL	160	350.000	0.03	18CDIP	AN0120NA
AN0120NA	N	OCTAL	200	300.000	0.03	18PDIP	AN0120NA
AN0120NB	N	OCTAL	200	300.000	0.04	18CDIP	AN0120NA

Supertex (continued)

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
AN0130NA	N	OCTAL	300	300.000	0.03	18PDIP	AN0130NA
AN0130NB	N	OCTAL	300	300.000	0.04	18CDIP	AN0130NA
AN0132NA	N	OCTAL	320	350.000	0.03	18PDIP	AN0140NA
AN0132NB	N	OCTAL	320	350.000	0.03	18CDIP	AN0140NA
AN0140NA	N	OCTAL	400	350.000	0.03	18PDIP	AN0140NA
AN0140NB	N	OCTAL	400	350.000	0.04	18CDIP	AN0140NA
AP0116NA	P	OCTAL	-160	700.000	-0.01	18PDIP	AP0120NA
AP0116NB	P	OCTAL	-160	700.000	-0.01	18CDIP	AP0120NA
AP0120NA	P	OCTAL	-200	600.000	-0.01	18PDIP	AP0120NA
AP0120NB	P	OCTAL	-200	600.000	-0.01	18CDIP	AP0120NA
AP0130NA	P	OCTAL	-300	600.000	-0.01	18PDIP	AP0130NA
AP0130NB	P	OCTAL	-300	600.000	-0.01	18CDIP	AP0130NA
AP0132NA	P	OCTAL	-320	700.000	-0.01	18PDIP	AP0140NA
AP0132NB	P	OCTAL	-320	700.000	-0.01	18CDIP	AP0140NA
AP0140NA	P	OCTAL	-400	700.000	-0.01	18PDIP	AP0140NA
AP0140NB	P	OCTAL	-400	700.000	-0.01	18CDIP	AP0140NA
TN0106N2	N		60	3.000	0.80	205AF	CF
TN0106N3	N		60	3.000	0.35	92	TN0106N3
TN0106ND	N		60	3.000	0.00	CHIP	TN0106ND
TN0110N2	N		100	3.000	0.80	205AF	CF
TN0110N3	N		100	3.000	0.50	92	TN0110N3
TN0110ND	N		100	3.000	0.00	CHIP	TN0110ND
TN0520N2	N		200	10.000	1.00	205AF	CF
TN0520N3	N		200	10.000	0.30	92	VN2410L
TN0520ND	N		200	10.000	0.00	CHIP	CF
TN0524N2	N		240	10.000	0.70	205AF	CF
TN0524N3	N		240	10.000	0.30	92	VN2410L
TN0524ND	N		240	10.000	0.00	CHIP	CF
TN0620N2	N		200	6.000	0.70	205AF	CF
TN0620N3	N		200	6.000	0.40	92	CF
TN0620ND	N		200	6.000	0.00	CHIP	CF
TN0624N2	N		240	6.000	0.70	205AF	CF
TN0624N3	N		240	6.000	0.40	92	CF
TN0624ND	N		240	6.000	0.00	CHIP	CF
VN0104N2	N		40	3.000	0.80	205AF	SD1117HD
VN0104N3	N		40	3.000	0.50	92	VN0104N3
VN0104N9	N		40	3.000	0.50	52	SD1117DD
VN0104ND	N		40	3.000	0.00	CHIP	VN0104ND
VN0106N2	N		60	3.000	0.80	205AF	SD1117HD
VN0106N3	N		60	3.000	0.50	92	VN0106N3
VN0106N9	N		60	3.000	0.50	52	SD1117DD
VN0106ND	N		60	3.000	0.00	CHIP	VN0106ND
VN0109N2	N		90	3.000	0.80	205AF	CF
VN0109N3	N		90	3.000	0.50	92	VN0109N3
VN0109N9	N		90	3.000	1.50	52	SD1107DD
VN0109ND	N		90	3.000	0.00	CHIP	VN0109ND
VN0110N2	N		100	8.000	0.50	205AF	SD1107HD
VN0110N3	N		100	8.000	0.30	92	SD1107BD
VN0114N2	N		140	8.000	0.50	205AF	SD1112HD
VN0114N3	N		140	8.000	0.30	92	SD1112BD
VN0116N2	N		160	10.000	0.35	205AF	SD1113HD
VN0116N3	N		160	10.000	0.25	92	SD1113BD
VN0116ND	N		160	10.000	0.00	CHIP	SD1113CHP
VN0120N2	N		200	10.000	0.35	205AF	SD1113HD
VN0120N3	N		200	10.000	0.25	92	SD1113BD

Supertex (continued)

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
VN0120ND	N		200	10.000	0.00	CHIP	SD1113CHP
VN0204N2	N		40	2.000	1.50	205AF	SD1117HD
VN0204ND	N		40	2.000	0.00	CHIP	SD1117CHP
VN0206N2	N		60	2.000	1.50	205AF	SD1117HD
VN0206N3	N		60	2.000	0.80	92	SD1117BD
VN0206ND	N		60	2.000	0.00	CHIP	SD1117CHP
VN0216N2	N		160	6.000	0.70	205AF	SD1112HD
VN0216N3	N		160	6.000	0.40	92	SD1112BD
VN0216ND	N		160	6.000	0.00	CHIP	SD1112CHP
VN0220N2	N		200	6.000	0.70	205AF	SD1112HD
VN0220N3	N		200	6.000	0.40	92	SD1112BD
VN0220ND	N		200	6.000	0.00	CHIP	SD1112CHP
VN0300B	N		30	1.200	1.86	205AF	SD3301HD
VN0300L	N		30	1.200	0.63	92	SD3301BD
VN0300M	N		30	1.200	0.75	237	SD3301AD
VN0530N2	N		300	50.000	0.25	205AF	SD1101HD
VN0530N3	N		300	50.000	0.10	92	SD1101BD
VN0530ND	N		300	50.000	0.00	CHIP	SD1101CHP
VN0535N2	N		350	35.000	0.25	205AF	SD1101HD
VN0535N3	N		350	35.000	0.10	92	SD1101BD
VN0535ND	N		350	35.000	0.00	CHIP	SD1101CHP
VN0540N2	N		400	35.000	0.25	205AF	SD1101HD
VN0540N3	N		400	35.000	0.10	92	SD1101BD
VN0540ND	N		400	35.000	0.00	CHIP	SD1101CHP
VN0545N2	N		450	60.000	0.10	205AF	CF
VN0545N3	N		450	60.000	0.05	92	SD1501BD
VN0545ND	N		450	60.000	0.00	CHIP	SD1501CHP
VN0550N3	N		500	60.000	0.05	92	SD1501BD
VN0550ND	N		500	60.000	0.00	CHIP	SD1501CHP
VN0606M	N		60	3.000	0.47	92	SD1117BD
VN0610L	N		60	5.000	0.19	92	VN0610LL
VN0808M	N		80	4.000	0.40	237	CF
VN10KN3	N		60	5.000	0.30	92	VN10KN3
VN10KN9	N		60	5.000	0.30	52	SD1106DD
VN1106N2	N		60	0.700	2.50	205AF	SD3301HD
VN1106ND	N		60	0.700	0.00	CHIP	SD3301CHP
VN1110N2	N		100	0.700	2.50	205AF	SD3300HD
VN1110ND	N		100	0.700	0.00	CHIP	SD3300CHP
VN1206B	N		120	6.000	0.63	205AF	CF
VN1206L	N		120	6.000	0.16	92	CF
VN1210B	N		120	10.000	0.40	205AF	CF
VN1210L	N		120	10.000	0.12	92	VN2410L
VN1304N2	N		40	8.000	0.40	205AF	SD1117HD
VN1304N3	N		40	8.000	0.25	92	SD1117BD
VN1304ND	N		40	8.000	0.00	CHIP	SD1117CHP
VN1306N2	N		60	8.000	0.40	205AF	SD1117HD
VN1306N3	N		60	8.000	0.25	92	SD1117BD
VN1306ND	N		60	8.000	0.00	CHIP	SD1117CHP
VN1310N2	N		100	8.000	0.40	205AF	SD1107HD
VN1310N3	N		100	8.000	0.25	92	SD1107BD
VN1310ND	N		100	8.000	0.00	CHIP	SD1107CHP
VN1316N2	N		160	40.000	0.15	205AF	SD1113HD
VN1316N3	N		160	40.000	0.10	92	SD1113BD
VN1316ND	N		160	40.000	0.00	CHIP	SD1113CHP
VN1320N2	N		200	40.000	0.15	205AF	SD1113HD

Supertex (continued)

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
VN1320N3	N		200	40.000	0.10	92	SD1113BD
VN1320ND	N		200	40.000	0.00	CHIP	SD1113CHP
VN1706B	N		170	6.000	0.63	205AF	CF
VN1706L	N		170	6.000	0.16	92	CF
VN1710B	N		170	10.000	0.60	205AF	CF
VN1710L	N		170	10.000	0.12	92	VN2410L
VN2010L	N		200	10.000	0.12	92	VN2410L
VN2106ND	N		60	3.000	0.00	CHIP	SD1117CHP
VN2110ND	N		100	3.000	0.00	CHIP	TN0110ND
VN2206ND	N		60	0.300	0.00	CHIP	CF
VN2210ND	N		100	0.300	0.00	CHIP	CF
VN2222L	N		60	7.500	0.15	92	VN2222LL
VN2406B	N		240	6.000	0.40	205AF	CF
VN2406L	N		240	6.000	0.25	92	CF
VN2410B	N		240	10.000	0.60	205AF	CF
VN2410L	N		240	6.000	0.12	92	VN2410L
VP0104N2	P		-40	8.000	-0.50	205AF	SD2107HD
VP0104N3	P		-40	8.000	-0.40	92	VP0104N3
VP0104ND	P		-40	8.000	0.00	CHIP	VP0104ND
VP0106N2	P		-60	8.000	-0.50	205AF	SD2107HD
VP0106N3	P		-60	8.000	-0.40	92	VP0106N3
VP0106ND	P		-60	8.000	0.00	CHIP	VP0106ND
VP0109N2	P		-90	8.000	-0.50	205AF	SD2107HD
VP0109N3	P		-90	8.000	-0.40	92	VP0109N3
VP0109ND	P		-90	8.000	0.00	CHIP	VP0109ND
VP0110N2	P		-100	16.000	0.00	205AF	SD2107HD
VP0110N3	P		-100	16.000	0.00	92	SD2107BD
VP0110ND	P		-100	16.000	0.00	CHIP	SD2107CHP
VP0204N2	P		-40	4.000	-0.80	205AF	SD2107HD
VP0204ND	P		-40	4.000	0.00	CHIP	SD2107CHP
VP0206N2	P		-60	4.000	-0.80	205AF	SD2107HD
VP0206N3	P		-60	4.000	-0.40	92	SD2107BD
VP0206ND	P		-60	4.000	0.00	CHIP	SD2107CHP
VP0210N2	P		-100	4.000	-0.80	205AF	SD2107HD
VP0210N3	P		-100	4.000	-0.40	92	SD2107BD
VP0210ND	P		-100	4.000	0.00	CHIP	SD2107CHP
VP0530N2	P		-300	100.000	0.00	205AF	CF
VP0530N3	P		-300	100.000	0.00	92	VP0540N3
VP0530ND	P		-300	100.000	0.00	CHIP	VP0540ND
VP0535N2	P		-350	75.000	-0.20	205AF	CF
VP0535N3	P		-350	75.000	-0.10	92	VP0540N3
VP0535ND	P		-350	75.000	0.00	CHIP	VP0540ND
VP0540N2	P		-400	75.000	-0.20	205AF	CF
VP0540N3	P		-400	75.000	-0.10	92	VP0540N3
VP0540ND	P		-400	75.000	0.00	CHIP	VP0540ND
VP0545N2	P		-450	125.000	-0.13	205AF	CF
VP0545N3	P		-450	125.000	-0.07	92	CF
VP0545ND	P		-450	125.000	0.00	CHIP	CF
VP0808B	P		-80	5.000	-0.88	205AF	SD2107HD
VP0808L	P		-80	5.000	-0.21	92	VP0808L
VP1008B	P		-100	5.000	-0.88	205AF	SD2107HD
VP1008L	P		-100	5.000	-0.21	92	VP1008L
VQ1000N6	N	QUAD	60	5.500	0.30	14PDIP	VQ1000J
VQ1000N7	N	QUAD	60	5.500	0.30	14CDIP	VQ1000J
VQ1004J	N	QUAD	60	3.500	0.46	14PDIP	SD1117N

Telmos

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
SD210CHP	N		30	70.000	0.00	CHIP	SD210CHP
SD210DE	N		30	70.000	0.05	72	SD210DE
SD210DE/R	N		30	70.000	0.05	72	SD210DE/R
SD211CHP	N	Z	30	70.000	0.00	CHIP	SD211CHP
SD211DE	N	Z	30	70.000	0.05	72	SD211DE
SD211DE/R	N	Z	30	70.000	0.05	72	SD211DE/R
SD212CHP	N		10	70.000	0.00	CHIP	SD212CHP
SD212DE	N		10	70.000	0.05	72	SD212DE
SD212DE/R	N		10	70.000	0.05	72	SD212DE/R
SD213CHP	N	Z	10	70.000	0.00	CHIP	SD213CHP
SD213DE	N	Z	10	70.000	0.05	72	SD213DE
SD213DE/R	N	Z	10	70.000	0.05	72	SD213DE/R
SD214CHP	N		20	70.000	0.00	CHIP	SD214CHP
SD214DE	N		20	70.000	0.05	72	SD214DE
SD214DE/R	N		20	70.000	0.05	72	SD214DE/R
SD215CHP	N	Z	20	70.000	0.00	CHIP	SD215CHP
SD215DE	N	Z	20	70.000	0.05	72	SD215DE
SD215DE/R	N	Z	20	70.000	0.05	72	SD215DE/R
SD5000CHP	N	Z QUAD	20	70.000	0.00	CHIP	SD5000CHP
SD5000J	N	Z QUAD	20	70.000	0.05	16CDIP	SD5000J
SD5000N	N	Z QUAD	20	70.000	0.05	16PDIP	SD5000N
SD5001CHP	N	Z QUAD	10	70.000	0.00	CHIP	SD5001CHP
SD5001J	N	Z QUAD	10	70.000	0.05	16CDIP	SD5001J
SD5001N	N	Z QUAD	10	70.000	0.05	16PDIP	SD5001N
SD5002CHP	N	Z QUAD	15	70.000	0.00	CHIP	SD5002CHP
SD5002J	N	Z QUAD	15	70.000	0.05	16CDIP	SD5002J
SD5002N	N	Z QUAD	15	70.000	0.05	16PDIP	SD5002N
SD5100CHP	N	Z QUAD	30	70.000	0.00	CHIP	SD5100CHP
SD5100N	N	Z QUAD	30	70.000	0.05	14PDIP	SD5100N
SD5101CHP	N	Z QUAD	15	70.000	0.00	CHIP	SD5101CHP
SD5101N	N	Z QUAD	15	70.000	0.05	14PDIP	SD5101N
SD5200CHP	N	Z QUAD	30	80.000	0.00	CHIP	SD5200CHP
SD5200N	N	Z QUAD	30	80.000	0.05	16PDIP	SD5200N
TMF123	N	DUAL	20	100.000	0.05	99	SD411HD

Texas Instruments

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
PV210	N		35	2.500	1.50	205AF	SD1117HD
PV211	N		60	3.500	1.50	205AF	SD1117HD
PV212	N		80	4.500	1.50	205AF	SD1117HD
TIS172	N		35	1.600	0.30	92	SD3301BD
TIS173	N		60	2.000	0.30	92	SD1117BD
TIS72	N		35	1.800	0.30	92	SD3301BD
TIS73	N		60	2.500	0.25	92	SD1117BD
TIS74	N		80	3.500	0.20	92	SD1107BD

Texet Semiconductor

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
TX101	N		60	6.000	0.80	92	SD1107BD
TX102	N		100	6.000	0.80	92	SD1107BD
TX103	N		150	12.000	0.40	92	SD1113BD
TX104	N		200	12.000	0.40	92	SD1113BD
TX105	N		350	40.000	0.25	92	SD1101BD
TX106	N		400	40.000	0.25	92	SD1101BD
TX107	N		450	70.000	0.20	92	SD1501BD
TX108	N		500	70.000	0.20	92	SD1501BD

Toshiba

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
2SK422	N		60	2.800	0.50	92	SD1117BD
2SK423	N		100	4.500	0.30	92	SD1107BD

Unitrode

PART NO.	CHAN.	DESCR.	(V) BV _{DSS}	(ohms) r _{DS(on)}	(Amps) I _{D(on)}	(TO-XX) PACKAGE	TOPAZ PART NUMBER
2N6781	N		60	0.600	3.50	205AF	2N6781
2N6782	N		100	0.600	3.50	205AF	2N6782
UFNF110	N		100	0.600	3.50	205AF	SD3300HD
UFNF111	N		60	0.600	3.50	205AF	SD3301HD
UFNF112	N		100	0.800	3.00	205AF	SD3300HD
UFNF113	N		60	0.800	3.00	205AF	SD3301HD
UFNF123	N		60	0.400	5.00	205AF	SD3301HD

N-Channel, Depletion-Mode, Lateral D-MOS FETs are suitable to replace N-Channel J-Fets under the following conditions:

- (1) A negative voltage is available to bias the Body (Substrate) of the D-MOS FET to the most negative point in the circuit.
- (2) The application requires faster switching speeds or wider operating bandwidth. J-FETs are still a better choice for low frequency applications where low 1/f Noise Voltage and low Gate Leakage below the I_G Breakpoint are the most important specifications.
- (3) The application is not low frequency and requires wider dynamic or higher I_G Breakpoint. Depletion-Mode Lateral D-MOS does not have an I_G Breakpoint by design and can operate in enhancement or depletion mode provided that rated breakdown voltages are not exceeded.

J-FET Industry Part No.	Depletion D-MOS Replacement	J-FET Industry Part No.	Depletion D-MOS Replacement
2N2606-09	—	FN4391-93	SD2100DE
2N3328-32	—	ITE4391-93	—
2N3382/84/86	—	PN4391-93	—
2N3684-87	—	SST4391-93	—
2N3819	—	2N4416	SD2100DE
2N3821-24	SD2100DE	ITE4416	—
2N3921-22	—	PN4416	—
2N3954-58	—	2N4856-61	SD2100DE
2N3954A-55A	—	2N4856A-61A	—
2N3970-72	SD2100DE	2N4867-69	—
2N3993-94	—	2N4867A-69A	—
2N4084-85	—	2N4978	—
2N4091-93	SD2100DE	2N5018-19	—
2N4091A-93A	SD2100DE	2N5045-47	—
ITE4091-93	—	2N5114-16	—
PN4091-93	—	PN5114-16	—
2N4117-19	—	PN5163	—
PN4117-19	—	2N5196-99	—
2N4117A-19A	—	2N5265-70	—
FN4117A-19A	—	2N5397-98	SD2100DE
PN4117A-19A	—	2N5432-34	—
2N4220-24	SD2100DE	PN5432-34	—
2N4220A-22A	SD2100DE	2N5452-54	—
2N4302-04	—	2N5457-59	—
PN4302-04	—	SST5457-59	—
2N4338-41	—	2N6460-65	—
PN4338-41	—	2N5484-86	—
2N4342-43	—	2N5515-24	—
2N4342-43	—	2N5545-47	—
2N4391-93	SD2100DE	DN5564-66	TZ5911HD

J-FET Industry Part No.	Depletion D-MOS Replacement
2N5564-66	TZ5911HD
2N5555	—
DN5567	TZ5911HD
2N5638-40	—
2N5653-54	—
2N5902-09	—
2N5911-12	TZ5911HD
IT5911-12	TZ5911HD
ITC5911-12	TZ5911HD
M5911-12	TZ5911HD
2N6483-85	—
2N6905-07	—
2N6908-11	—
CR022-430	—
CRR0240-4300	—
DPAD series	—
IT100-01	—
IT500-05	—
IT550	TZ5911HD
Jxxx series	—
M440-441	TZ5911HD
MPF series	—
PAD series	—
U200-202	—
U231-235	—
U257	TZ5911HD
U290-91	—
U304-306	SD2200DE
U308-310	SD2200DE
U311	SD2200DE
U320-322	—
U350	SD5501N
U401-06	—
U410-12	—
U420-26	—
U427-28	—
U430-31	TZ5911HD
U440-42	TZ5911HD
U443-44	TZ5911HD
U1897-99	—
VCR series	—

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION

TO-205 AF (TO-18)	TO-205	TO-205
Power Package	Power	Power
Description	100V 0.5 Amp	60V 1.0 Amp

FEATURES

- Gate Stand-off Voltage, $\pm 40V$ min.
- Continuous I_D of 1 Amp in small package
- Wide Variety of Packages

APPLICATIONS

- Motor Controls
- Line Drivers
- Power Supplies

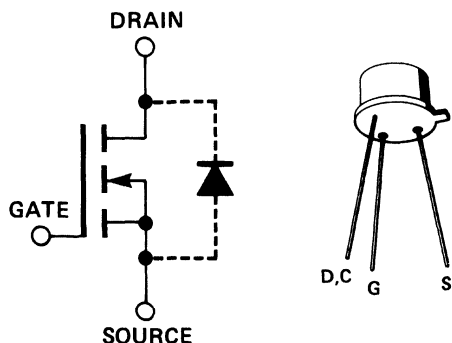
ABSOLUTE MAXIMUM RATINGS ($T_C = +25^\circ C$ unless otherwise noted)

Drain-Source Voltage		
2N6782	100V*	
2N6781	60V*	
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)		
2N6782	100V*	
2N6781	60V*	
Gate-Source Voltage	$\pm 40V$	
Continuous Drain Current		
	$T_C = +100^\circ C$	$T_C = +25^\circ C$
	2.25A*	3.5A*
Peak Pulsed Drain Current	8.0A	

Maximum Power Dissipation		
	$T_C = +100^\circ C$	$T_C = +25^\circ C$
	6.0W*	15W*
Linear Derating Factor		
	Junction to Ambient	Junction to Case
	(mW/ $^\circ C$)	(mW/ $^\circ C$)
	5.0*	120*
Operating Junction and Storage		
Temperature Range	-55 to +150 $^\circ C$ *	
Lead Temperature (1/16" from mounting surface for 30 Sec)	+300 $^\circ C$ *	

*JEDEC Registered Values

CONFIGURATION



PACKAGE DIMENSIONS

TO-205 AF
(See Package 6)

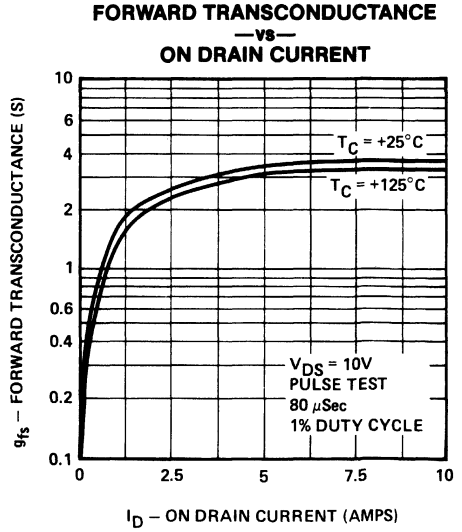
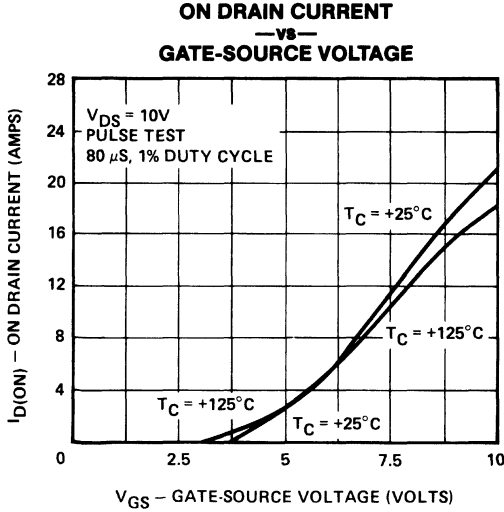
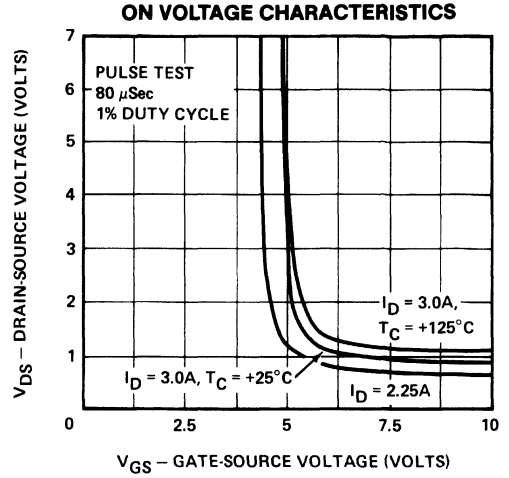
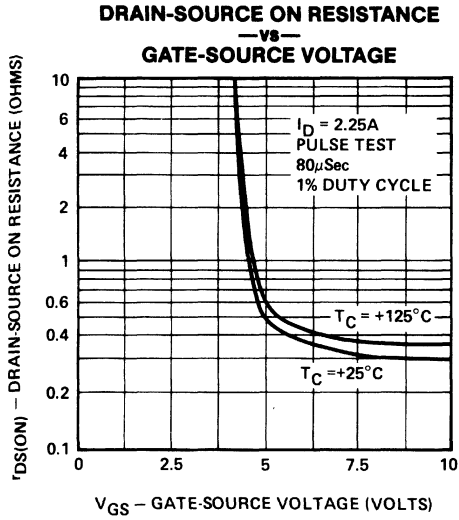
ELECTRICAL CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC	2N6782			2N6781			UNIT	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
1	BV_{DSS} Drain-Source Breakdown Voltage	100*	125		60*	90		V	$I_D = 250\mu\text{A}, V_{GS} = 0$
2	$V_{GS(th)}$ Gate-Source Threshold Voltage	2.0*		4.0*	2.0*		4.0*	V	$V_{DS} = V_{GS}$ $I_D = 250\mu\text{A}$ $T_C = +125^\circ\text{C}$
3		1.0*		4.0*	1.0*		4.0*		
4	I_{GBS} Gate-Body Leakage Current			100*			100*	nA	$V_{GS} = 20\text{V}, V_{DS} = 0$ $T_C = +125^\circ\text{C}$
5				200*			200*		
6				-100*			-100*		
7	I_{DSS} Drain-Source OFF Leakage Current			0.25*				mA	$V_{GS} = -20\text{V}, V_{DS} = 0$ $T_C = +125^\circ\text{C}$
8				1.0*					
9							0.25*		
10							1.0*		
11	$I_{D(on)}$ ON Drain Current ⁽¹⁾	3.5*			3.5*			A	$V_{DS} = 10\text{V}, V_{GS} = 10\text{V}$
12	$V_{DS(on)}$ Drain-Source ⁽¹⁾ ON Voltage			2.1*			2.1*	V	$V_{GS} = 10\text{V}, I_D = 3.5\text{A}$
13	$r_{D(on)}$ Drain-Source ⁽¹⁾ ON Resistance			0.6*			0.6*	ohms	$V_{GS} = 10\text{V}$ $I_D = 2.25\text{A}$ $T_C = +125^\circ\text{C}$
14				1.08*			1.08*		
15	g_{fs} Common-Source ⁽¹⁾ Forward Transcond.	1.0*		3.0*	1.0*		3.0*	S	$V_{DS} = 10\text{V}, V_{GS} = 10\text{V}$ $f = 1\text{KHz}$
16	C_{iss} Common-Source Input Capacitance	60*		200*	60*		200*	pF	$V_{DS} = 25\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$
17	C_{ras} Common-Source Reverse Transfer Capacitance	10*		25*	10*		25*		
18	C_{oss} Common-Source Output Capacitance	40*		100*	40*		100*		
19	$t_{d(on)}$ Turn-ON Delay Time			15*			15*	nsec	$V_{DD} = 34\text{V}$ $R_L = 15\text{ ohms}$ $R_G = 25\text{ ohms}$ $V_{G(on)} = 10\text{V}$
20	t_r Rise Time			25*			25*		
21	$t_{d(off)}$ Turn-OFF Delay Time			25*			25*		
22	t_f Fall Time			20*			20*		
23	I_S Continuous Source Current ⁽¹⁾	3.5*			3.5*			A	
24	I_{SM} Peak Source Current ⁽¹⁾	8.0*			8.0*				
25	V_{SD} Source-Drain ⁽¹⁾ Forward Voltage	0.75*		1.50*	0.75*		1.50*	V	$V_{GS} = 0, I_S = 3.5\text{A}$
26	$R_{th J-C}$ Thermal Resistance Junction-to-Case			8.33*			8.33*	$^\circ\text{C/W}$	
27	$R_{th J-A}$ Thermal Resistance Junction-to-Ambient			170			170	$^\circ\text{C/W}$	

Note 1: Pulse Test 80 μSec , 1% Duty Cycle

*JEDEC Registered Values

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)



N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION

2N7000	2N7000
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FEATURES

- High Gate Oxide Breakdown, $\pm 40V$ min.
- Low Output and Transfer Capacitances
- Extended Safe Operating Area

APPLICATIONS

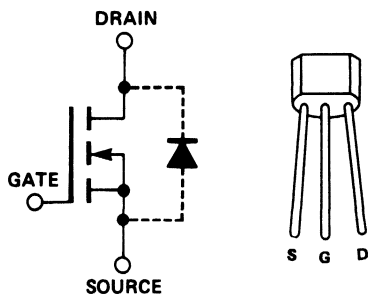
- High-Speed Pulse Amplifiers
- Logic Buffers
- Line Drivers
- Solid-State Relays
- Motor Controls
- Power Supplies

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ C$ unless otherwise noted)

Drain-Source Voltage	+60V	
Drain-Gate Voltage ($V_{GS} = 0$)	+60V	
Gate-Source Voltage	$\pm 40V$	
Continuous Drain Current	$T_A = 25^\circ C$	$T_C = 25^\circ C$
	.21A	.32A
Peak Pulsed Drain Current	0.79A	

Continuous Device Dissipation	400mW
Linear Derating Factor	3.2mW/ $^\circ C$
Pulsed Device Dissipation	3.125W
Linear Derating Factor	25mW/ $^\circ C$
Operating Junction Temperature Range	-55 to +150 $^\circ C$
Storage Temperature Range	-55 to +150 $^\circ C$
Lead Temperature (1/16" from mounting surface for 30 Sec)	+300 $^\circ C$

SCHEMATIC DIAGRAM/PACKAGE



PACKAGE DIMENSIONS (TO-92) TO-226AA

(See Package 5)

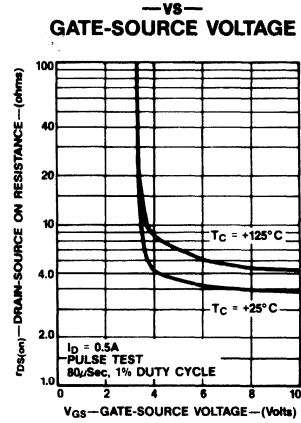
ELECTRICAL CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC	2N7000			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
1	BV_{DSS} Drain-Source Breakdown Voltage	60	100		V	$I_D = 10\mu\text{A}$, $V_{GS} = 0$
2	$V_{GS(th)}$ Gate-Source Threshold Voltage	0.8	1.9	3.0	V	$I_D = 1.0\text{mA}$, $V_{DS} = V_{GS}$
3	I_{GBS} Gate-Body Leakage Current		± 1.0	± 10	nA	$V_{GS} = \pm 15\text{V}$, $V_{DS} = 0$
4	I_{DSS} Drain-Source OFF Leakage Current		0.1	1.0	μA	$V_{DS} = 48\text{V}$, $V_{GS} = 0$
5			.01	1.0	mA	$T_C = +125^\circ\text{C}$
6	$I_{D(on)}$ ON Drain Current	75			mA	$V_{DS} = 10\text{V}$, $V_{GS} = 4.5\text{V}$ (Note 1)
7	$V_{DS(on)}$ Drain-Source ON Voltage			0.4		$V_{GS} = 4.5\text{V}$, $I_D = 75\text{mA}$ (Note 1)
8			1.5	2.5	V	$V_{GS} = 10\text{V}$, $I_D = 0.5\text{A}$ (Note 1)
9	$r_{DS(on)}$ Drain-Source ON Resistance		3.0	5.0	ohms	$V_{GS} = 10\text{V}$, $I_D = 0.5\text{A}$ (Note 1)
10			4.7	9.0		$T_C = +125^\circ\text{C}$
11	g_{fs} Common-Source Forward Transcond.	100			mmhos	$V_{DS} = 10\text{V}$, $I_D = 0.2\text{A}$ $f = 1\text{KHz}$ (Note 1)
12	C_{iss} Common-Source Input Capacitance			60		
13	C_{rss} Common-Source Reverse Transfer Capacitance		1.3	5.0	pF	$V_{DS} = V_{GS} = 0$ $f = 1\text{MHz}$
14	C_{oss} Common-Source Output Capacitance		10.5	25		
15	t_{on} Turn-On Time		5.0	10	nSec	$V_{DD} = 15\text{V}$, $V_{G(on)} = 10\text{V}$
16	t_{off} Turn-Off Time		6.0	10		$R_G = 25\Omega$, $R_L = 25\Omega$

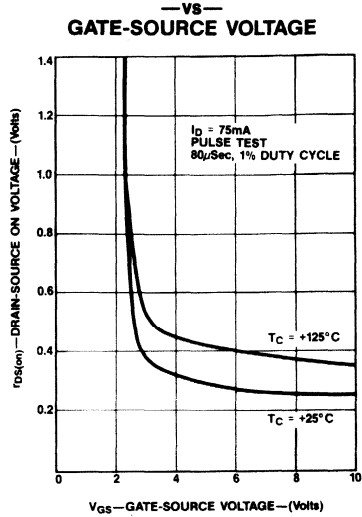
Note 1: Pulse Test $80\mu\text{Sec}$, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise specified)

DRAIN-SOURCE ON RESISTANCE

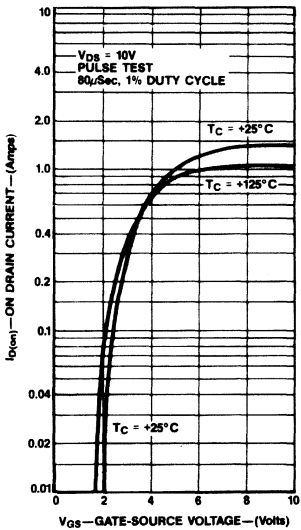


DRAIN-SOURCE ON VOLTAGE



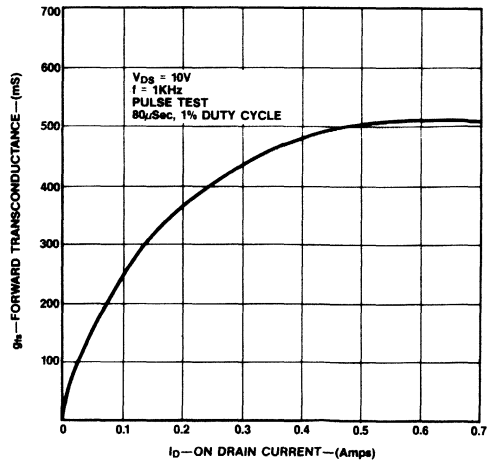
ON DRAIN CURRENT

—VS—
GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE

—VS—
ON DRAIN CURRENT



TOPAZ SEMICONDUCTOR

2N7104, 2N7105, 2N7106 2N7107, 2N7108, 2N7109

N-CHANNEL ENHANCEMENT-MODE D-MOS FET SWITCHES

ORDERING INFORMATION

TO-226AF (TO-72) PACKAGE SHORTING RINGS ON LEADS		2N7104	2N7105+	2N7106	2N7107+	2N7108	2N7109+
Sorted chips in Wafer Pack		SD210CHP	SD211CHP	SD212CHP	SD213CHP	SD214CHP	SD215CHP
DESCRIPTION	V_{DS} min.	30V	30V	10V	10V	20V	20V
	V_{SB} min.	10V	10V	10V	10V	20V	20V
	f_{gate} max.	70 ohms	70 ohms	70 ohms	70 ohms	70 ohms	70 ohms

+ Gate Protective Diode

FEATURES

- High Input to Output Isolation—120dB typical
- Low feedthrough and feedback transients
- Low inter-electrode Capacitances

APPLICATIONS

- +30V Switch Drivers—2N7104, 2N7105
- $\pm 10V$ Analog Switches—2N7108, 2N7109
- $\pm 5V$ Analog Switches—2N7106, 2N7107

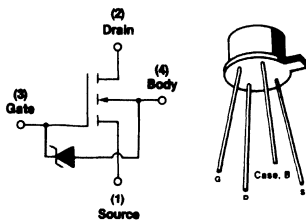
ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

PARAMETER	2N 7104	2N 7105	2N 7106	2N 7107	2N 7108	2N 7109	UNIT
Breakdown Voltages							
V _{DS}	+30	+30	+10	+10	+20	+20	V
V _{SD}	+10	+10	+10	+10	+20	+20	V
V _{DB}	+30	+30	+15	+15	+25	+25	V
V _{SB}	+15	+15	+15	+15	+25	+25	V
V _{GS}	$\pm 40^*$	-15	$\pm 40^*$	-15	$\pm 40^*$	-25	V
		+25		+25		+30	V
V _{GB}	± 40	-0.3	± 40	-0.3	± 40	-0.3	V
		+25		+25		+30	V
V _{GD}	± 40	-30	± 40	-15	± 40	-25	V
		+25		+25		+30	V
V _{DG}	+40*	+25*	+40*	+25*	+40*	+30*	V

I _D	Continuous Drain Current	50mA*
P _T	Power Dissipation (at or below T _c = +25°C)	1.2W
	Linear Derating Factor	12mW/°C
P _D	Power Dissipation (at or below T _A = +25°C)	300mW*
	Linear Derating Factor	2.4 mW/°C*
T _J	Operating Junction Temperature Range	-55 to +150°C*
T _S	Storage Temperature Range	-65 to +200°C
T _L	Lead Temperature (1/16" from mounting surface for 10 sec)	+300°C

*JEDEC Registered Value

SCHEMATIC DIAGRAM

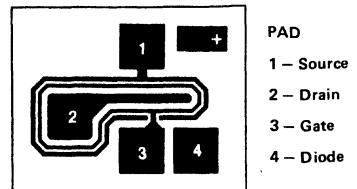


Body Internally connected to Case.
Diode protection on 2N7105/2N7107/2N7109

PACKAGE DIMENSIONS

TO-72
(See Package 3)

CHIP CONFIGURATION



For SD211/213/215 CHP, bond Gate and Diode to common point. Body is backside contact.
Dimensions: .022x.025x.013 Inches

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#	PARAMETER		2N7104, 2N7105			2N7106, 2N7107			2N7108, 2N7109			UNIT	TEST CONDITIONS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
1	BV _{DS}	Drain-Source Breakdown Voltage	30	35							V	I _D = 10μA V _{GS} = V _{BS} = 0	
2			10	25		10	25		20	25		I _D = 10nA V _{GS} = V _{BS} = -5V	
3	I _{LOSS}	Zero Gate Voltage Drain Current			10*						μA	V _{DS} = 30V V _{GS} = V _{BS} = 0	
4	BV _{SD}	Source-Drain Breakdown Voltage	10			10			20		V	I _S = 10nA V _{GD} = V _{BD} = -5.0V	
5	BV _{DB}	Drain-Substrate Breakdown Voltage	15			15			25			I _D = 10nA, V _{GB} = 0 Source OPEN	
6	BV _{SB}	Source-Substrate Breakdown Voltage	15			15			25			I _S = 10μA, V _{GB} = 0 Drain OPEN	
7	I _{D (off)}	Drain-Source OFF Current			10*			10*			nA	V _{DS} = 10V V _{GS} = V _{BS} = -5V	
8										10*		V _{DS} = 20V	
9						5.0*			5.0*			μA	V _{DS} = 10V V _{GS} = V _{BS} = -5V T _A = +125°C
10									5.0*	V _{DS} = 20V			
11	I _{S (off)}	Source-Drain OFF Current			10*			10*			nA	V _{SD} = 10V V _{GD} = V _{BD} = -5V	
12										10*		V _{SD} = 20V	
13						5.0*			5.0*			μA	V _{SD} = 10V V _{GD} = V _{BD} = -5V T _A = +125°C
14									5.0*	V _{SD} = 20V			
15	I _{GSS}	Gate Reverse Current	2N7104		0.1*						nA	V _{GS} = 12V	
16			2N7106					0.1*				μA	V _{GS} = 25V
17			2N7108							0.1*			V _{GS} = 30V
18			2N7105			1.0*						μA	V _{GS} = 12V
19			2N7107					1.0*					V _{GS} = 25V
20			2N7109							1.0*			V _{GS} = 30V
21			2N7104			1.0*						μA	V _{GS} = 12V
22			2N7106					1.0*					V _{GS} = 25V
23			2N7108							1.0*			V _{GS} = 30V
24	2N7105			100*						μA	V _{GS} = 12V		
25	2N7107					100*					V _{GS} = 25V		
26	2N7109							100*			V _{GS} = 30V		
27	V _{GS(th)}	Gate Threshold Voltage	0.5*	1.0	2.0*	0.1*	1.0	2.0*	0.1*	1.0	2.0*	V	V _{DS} = V _{GS} , I _D = 1μA, V _{SB} = 0
28	r _{DS(on)}	Drain-Source ON Resistance		50	70*		50	70*		50	70*	ohms	V _{GS} = 5V I _D = 1mA
29				30	45		30	45		30	45		V _{GS} = 10V V _{SB} = 0

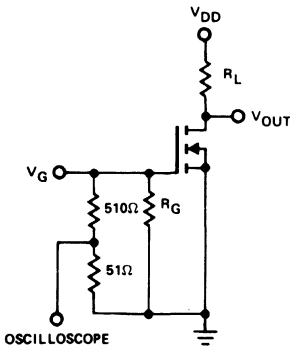
*JEDEC Registered Value

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted), continued

#	PARAMETER	2N7104, 2N7105			2N7106, 2N7107			2N7108, 2N7109			UNIT	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
30	g_{fs} Common-Source Forward Transcond.	10	12		10	12		10	12		mmhos	$V_{DS} = 10\text{V}$, $I_D = 20\text{mA}$, $f = 1\text{KHz}$, $V_{SB} = 0$
31	C_{iss} Input Capacitance		2.4	3.5*		2.4	3.5*		2.4	3.5	pF	$V_{DS} = 10\text{V}$ $V_{GS} = V_{BS} = -15\text{V}$ $f = 1\text{MHz}$
32	$C_{i(gd + db)}$ Drain Node Capacitance		1.3	1.5		1.3	1.5		1.3	1.5		
33	$C_{i(gs + sb)}$ Source Node Capacitance		3.5	4.0		3.5	4.0		3.5	4.0		
34	C_{rss} Reverse Transfer Capacitance		0.3	0.5*		0.3	0.5*		0.3	0.5*		
35	$t_{d(on)}$ Turn ON Delay Time		0.7	1.0*		0.7	1.0*		0.7	1.0*	nSec	$V_{DD} = 5\text{V}$, $V_{G(on)} = 5\text{V}$ $R_L = 680\Omega$, $R_G = 51\Omega$
36	t_r Rise Time		0.8	1.0*		0.8	1.0*		0.8	1.0*		
37	t_{off} Turn OFF Time		10			10			10			

*JEDEC Registered Value

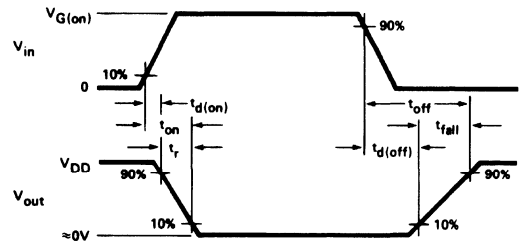
SWITCHING TIMES TEST CIRCUIT



INPUT PULSE
 $t_r < 0.5 \text{ nSEC}$
 PULSE WIDTH – 100 nSEC

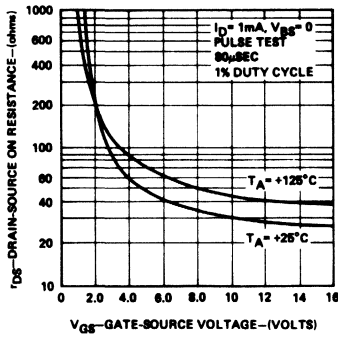
SAMPLING OSCILLOSCOPE
 $t_r < 0.36 \text{ nSEC}$
 $R_{in} > 1\text{M}\Omega$
 $C_{in} < 2.0 \text{ pF}$

TEST WAVEFORMS

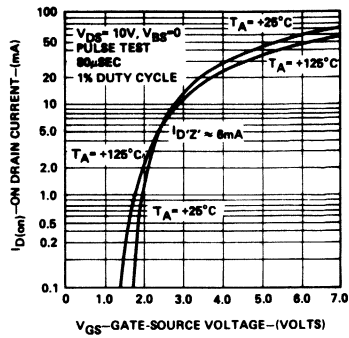


TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

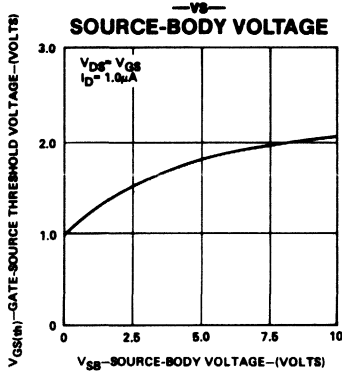
DRAIN-SOURCE ON RESISTANCE
—VS—
GATE-SOURCE VOLTAGE



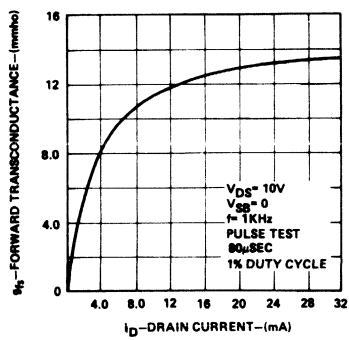
ON DRAIN CURRENT
—VS—
GATE-SOURCE VOLTAGE



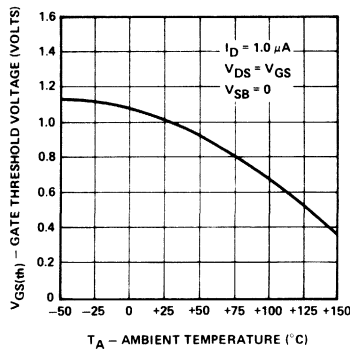
GATE-SOURCE THRESHOLD VOLTAGE



FORWARD TRANSCONDUCTANCE
—VS—
ON DRAIN CURRENT



GATE THRESHOLD VOLTAGE
—VS—
AMBIENT TEMPERATURE



N-CHANNEL ENHANCEMENT MODE D-MOS FETs 8-CHANNEL ARRAYS

ORDERING INFORMATION

18 Pin Plastic DIP	ANO110N	ANO120N	ANO130N	ANO140N
Description (each channel)	100V,100Ω	200V,300Ω	300V,300Ω	400V,300Ω

FEATURES

- Ultra-Low Channel OFF Leakage, <800pA
- High Channel-to-Channel Isolation
- 100V to 400V Capability
- Industry Standard Pin-Out

APPLICATIONS

- Electrostatic Array Drivers
- Electroluminescent Panel Drivers
- Converters
- Multi-Channel Array Drivers

ABSOLUTE MAXIMUM RATINGS (T_A = +25 °C per channel unless otherwise specified)

Drain-Source Voltage

ANO110N	+100V
ANO120N	+200V
ANO130N	+300V
ANO140N	+400V

Drain-Gate Voltage (V_{GS} = 0)

ANO110N	+100V
ANO120N	+200V
ANO130N	+300V
ANO140N	+400V

Channel-to-Channel Isolation Voltage

Drain-to-Drain Voltage (V _{GS} = 0)	
ANO110N	+100V
ANO120N	+200V
ANO130N	+300V
ANO140N	+400V

Gate-Source Voltage

±30V

Operating and Storage Temperature

Range -55 to +85 °C

Lead Temperature (1/16" from mounting

Surface for 10 sec.) +300 °C

Continuous Drain Current, Total Package

	T _A = +25 °C	T _C = +25 °C
ANO110N	80mA	140mA
ANO120N, ANO130N	50mA	80mA
ANO140N	40mA	75mA

Continuous Drain Current, Single Channel

	T _A = +25 °C	T _C = +25 °C
ANO110N	50mA	100mA
ANO120N, ANO130N	30mA	60mA
ANO140N	25mA	50mA

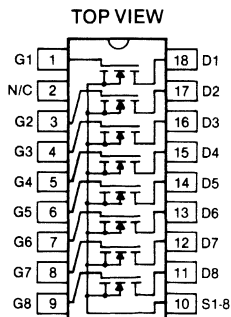
Continuous Device Dissipation

	T _A = +25 °C	T _C = +25 °C
Total Package	.64W	2.0W
Single Channel	.30W	1.0W

Linear Derating Factor

	T _A = +25 °C	T _C = +25 °C
Total Package	10.67mW/°C	33.2mW/°C
Single Channel	5mW/°C	16.6mW/°C

PIN CONFIGURATION & SCHEMATIC DIAGRAM



PACKAGE DIMENSIONS

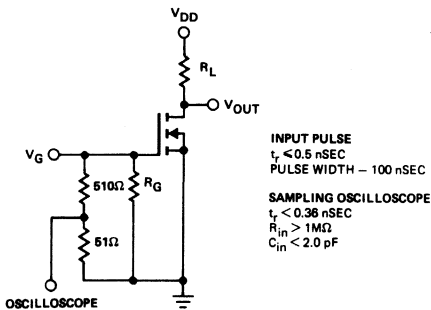
18-Pin Plastic DIP
(See Package 11)

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ per channel unless otherwise noted)

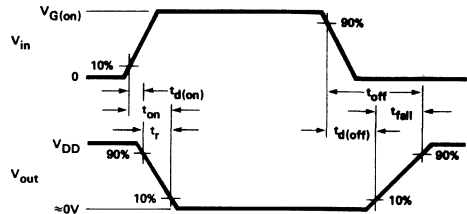
#	CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITIONS	
1	BV _{DSS}	Drain-Source Breakdown Voltage	AN0110	100	160	V	I _D = 100 μ A, V _{GS} = 0	
2			AN0120	200	300			
3			AN0130	300	400			
4			AN0140	400	450			
5	I _{DSS}	Drain-Source OFF Leakage Current	AN0110		5.0	nA	V _D S = 80V	V _G S = 0 (NOTE 1)
6			AN0120		5.0			
7			AN0130		5.0			
8			AN0140		5.0			
9	I _{GBS}	Gate-Body Leakage Current			10	nA	V _G S = 20V, V _D S = 0	
10	V _{GS(th)}	Gate-Source Threshold Voltage	2.0		5.0	V	V _D S = V _G S, I _D = 1.0mA	
11	r _{DS(on)}	Drain-Source ON Resistance	AN0110	60	100	ohms	I _D = 10mA, V _G S = 10V	
12			AN0120	210	300			
13			AN0130	260	300			
14			AN0140	325	350			
15	I _{D(on)}	Drain-Source ON Current	AN0110	50		mA	V _D S = 25V, V _G S = 10V	
16			AN0120	25				
17			AN0130	25				
18			AN0140	25				
19	g _{fs}	Common-Source Forward Transcond	AN0110	8.0		mmhos	V _D S = 25V, I _D = 10mA, f = 1KHz	
20			AN0120	4.0				
21			AN0130	4.0				
22			AN0140	4.0				
23	c _{iss}	Common-Source Input Capacitance		8.0	10	pF	V _D S = 25V, V _G S = 0, f = 1MHz	
24	c _{oss}	Common-Source Output Capacitance		1.5	2.0			
25	c _{rss}	Common-Source Reverse Transfer Capacitance		0.8	1.0			
26	t _{d(on)}	Turn-ON Delay Time		3		nS	V _{DD} = 25V, V _{G(on)} = 10V R _L = 820 Ω R _G = 51 Ω	
27	t _r	Rise Time		3				
28	t _{d(off)}	Turn-OFF Delay Time		5				
29	t _f	Fall Time		5				

Note 1: Limit is OFF leakage of all 8 segments in parallel.

SWITCHING TIMES TEST CIRCUIT

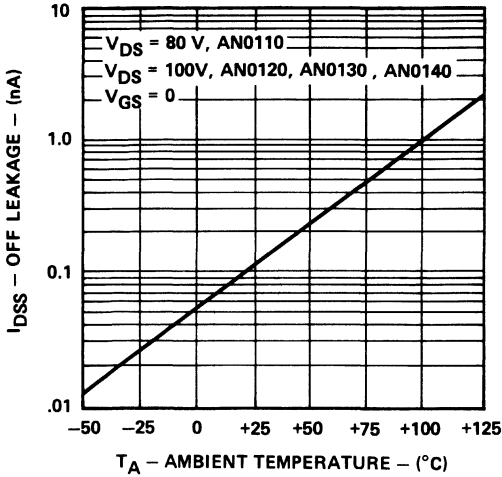


TEST WAVEFORMS

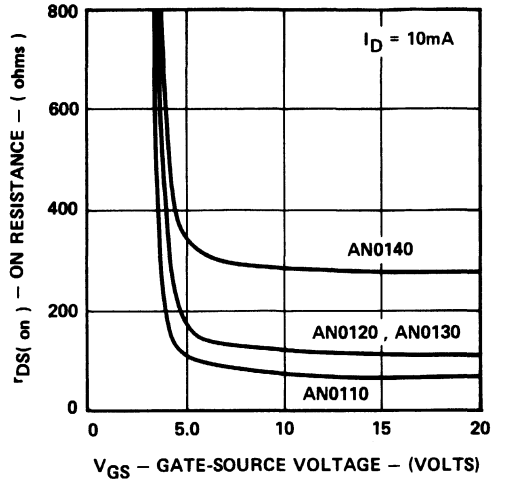


TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$, per channel, unless otherwise specified)

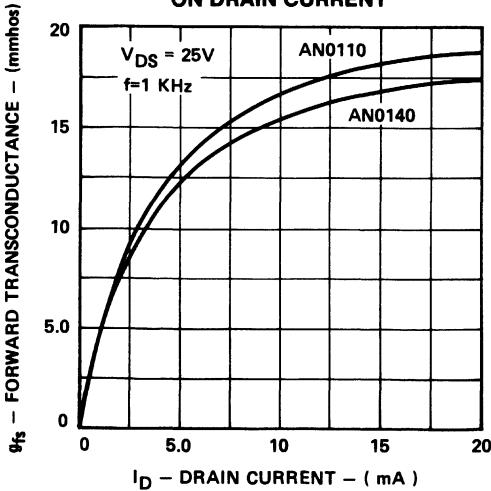
DRAIN-SOURCE OFF LEAKAGE
—VS—
AMBIENT TEMPERATURE



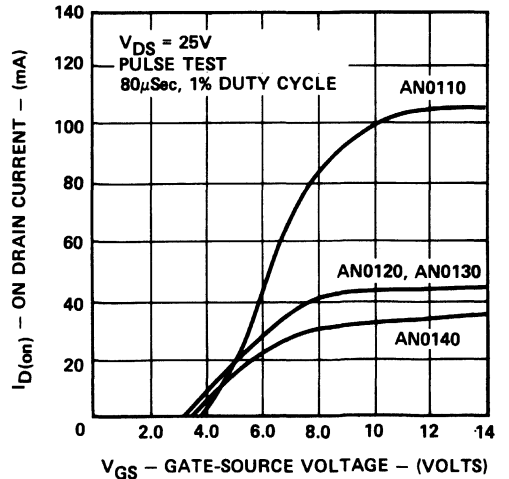
DRAIN-SOURCE ON RESISTANCE
—VS—
GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE
—VS—
ON DRAIN CURRENT



ON DRAIN CURRENT
—VS—
GATE-SOURCE VOLTAGE



P-CHANNEL ENHANCEMENT MODE D-MOS FETs 8-CHANNEL ARRAYS

ORDERING INFORMATION

18 Pin Plastic DIP	AP0120NA	AP0130NA	AP0140NA
Drain-Source (each channel)	-200V, 600Ω	-300V, 900Ω	-400V, 700Ω

FEATURES

- Ultra-Low Channel OFF Leakage, <-800pA
- High Channel-to-Channel Isolation
- N-Channel Complements available
- Industry Standard Pin-Out

APPLICATIONS

- Electrostatic Array Drivers
- Electroluminescent Panel Drivers
- Converters
- Multi-Channel Array Drivers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C per channel, unless otherwise specified)

Drain-Source Voltage

AP0120N	-200V
AP0130N	-300V
AP0140N	-400V

Drain-Gate Voltage (V_{GS} = 0)

AP0120N	-200V
AP0130N	-300V
AP0140N	-400V

Channel-to-Channel Isolation Voltage

Drain-to-Drain Voltage (V_{GS} = 0)

AP0120N	-200V
AP0130N	-300V
AP0140N	-400V

Gate-Source Voltage

Operating and Storage Temperature

Range -55 to +85°C

Lead Temperature (1/16" from mounting

Surface for 10 sec.) +300°C

Continuous Drain Current, Total Package

	T _A = +25°C	T _C = +25°C
AP0120N, AP0130N	-25mA	-40mA
AP0140N	-20mA	-35mA

Continuous Drain Current, Single Channel

	T _A = +25°C	T _C = +25°C
AP0120N, AP0130N, AP0140N	-15mA	-25mA

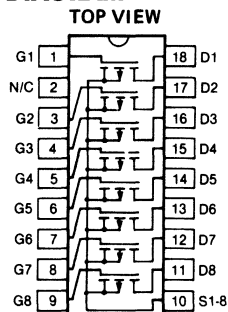
Continuous Device Dissipation

	T _A = +25°C	T _C = +25°C
Total Package	.64W	2.0W
Single Channel	.30W	1.0W

Linear Derating Factor

	T _A = +25°C	T _C = +25°C
Total Package	10.67mW/°C	33.2mW/°C
Single Channel	5mW/°C	16.6mW/°C

PIN CONFIGURATION & SCHEMATIC DIAGRAM



PACKAGE DIMENSIONS

18-Pin Plastic DIP

(See Package 11)

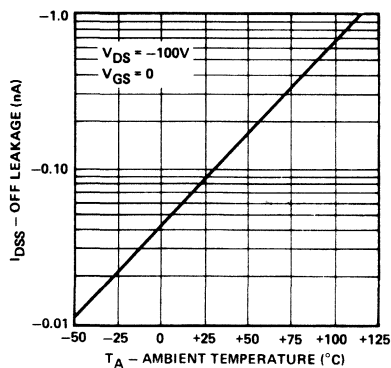
ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ per channel unless otherwise noted)

#	CHARACTERISTIC			MIN	TYP	MAX	UNIT	TEST CONDITIONS
1	BV _{DSS}	Drain-Source Breakdown Voltage	AP0120N	-200			V	I _D = -100 μ A, V _{GS} = 0
2			AP0130N	-300				
3			AP0140N	-400				
4	I _{DSS}	Drain-Source OFF Leakage Current			-5.0	nA	V _{DS} = -100V, V _{GS} = 0 (NOTE 1)	
5	I _{GBS}	Gate-Body			± 10	nA	V _{GB} = ± 20 V, V _{DS} = 0	
6		Leakage Current			± 1.0	μ A	V _{GB} = ± 40 V, V _{DS} = 0	
7	V _{GS(th)}	Gate-Source Threshold Voltage		-2.0		-5.0	V	V _{DS} = V _{GS} , I _D = -0.5mA
8	r _{DS(on)}	Drain-Source	AP0120N, AP0130N			600	ohms	I _D = -10mA, V _{GS} = -10V
9		ON Resistance	AP0140N			700		
10	I _{D(on)}	Drain-Source ON Current		-15			mA	V _{DS} = -25V, V _{GS} = -10V
11	g _{fs}	Common-Source Forward Transconductance		3.0			mmhos	V _{DS} = -25V, I _D = -5mA f = 1KHz
12	C _{iss}	Common-Source Input Capacitance			8.0	10	pF	V _{DS} = -25V, V _{GS} = 0, f = 1MHz
13	C _{OSS}	Common-Source Output Capacitance			1.5	2.0		
14		Common-Source Reverse Transfer Capacitance			0.8	1.0		
15	t _{d(on)}	Turn-ON Delay Time			6		nS	V _{DD} = -25V, V _{G(on)} = -10V R _L = 500 Ω R _G = 51 Ω
16	t _r	Rise time			6			
17	t _{d(off)}	Turn-OFF Delay Time			8			
18	t _f	Fall Time			6			

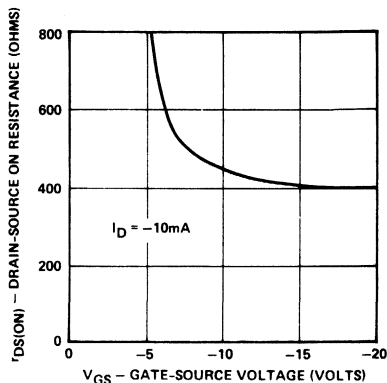
Note 1: Limit is OFF leakage of all 8 segments in parallel.

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$, per channel, unless otherwise specified)

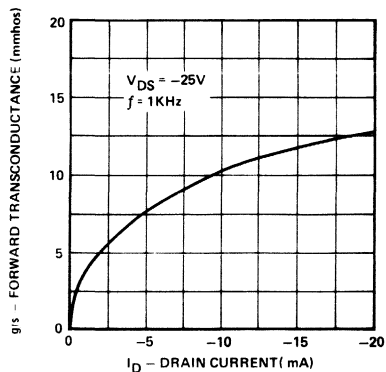
DRAIN-SOURCE OFF LEAKAGE
—vs—
AMBIENT TEMPERATURE



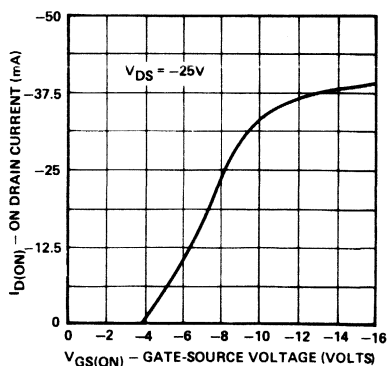
DRAIN-SOURCE ON RESISTANCE
—vs—
GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE
—vs—
ON DRAIN CURRENT



ON DRAIN CURRENT
—vs—
GATE-SOURCE VOLTAGE



N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FET

ORDERING INFORMATION

TO-92 Plastic Package	BS170
Description	60V, 3.0mA

FEATURES

- Reliable, low cost, plastic package
- European TO-92 pin-out
- Low capacitance

APPLICATIONS

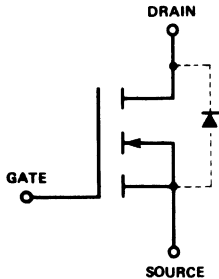
- High-Speed Pulse Amplifiers
- Logic Buffers
- Line Drivers

ABSOLUTE MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

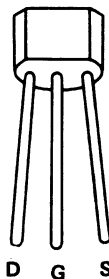
Drain-Source Voltage	60V	
Drain-Gate Voltage (R _{GS} = 1MΩ)	60V	
Gate-Source Voltage	±30V	
Continuous Drain Current	T _C = +100°C	T _C = +25°C
	.21A	.32A
Peak Pulsed Drain Current	1.0A	
Maximum Power Dissipation	T _C = +100°C	T _C = +25°C
	0.4	3.0

Linear Derating Factor	Junction to Ambient (mW/°C)	Junction to Ambient (mW/°C)
	3.0	24
Operating Junction and Storage Temperature Range	-55°C to +150°C	
Lead Temperature (1/16" from mounting surface for 30 Sec)	+260°C	

SCHEMATIC DIAGRAM



TO-92



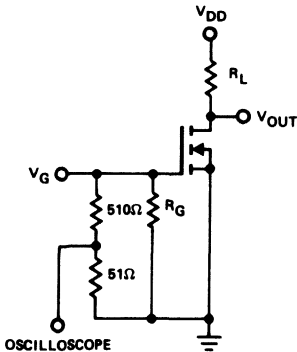
PACKAGE DIMENSIONS TO-226AA (TO-92)

(See Package 5)

ELECTRICAL CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS
1	BV _{DSS}	Drain Source Breakdown Voltage	60	100		V	$I_D = 100\mu\text{A}$, $V_{GS} = 0$
2	V _{GS(th)}	Gate Source Threshold Voltage	0.8	2.1	3.0	V	$V_{DS} = V_{GS}$, $I_D = 1\text{mA}$
3	I _{GSSF}	Gate Body Forward Leakage Current		.03	10	nA	$V_{GS} = 20\text{V}$, $V_{DS} = 0$
4	I _{GSSR}	Gate Body Reverse Leakage Current		-.06	-10		$V_{GS} = -20\text{V}$, $V_{DS} = 0$
5	I _{DSS}	Drain-Source OFF Leakage Current			0.5	μA	$V_{DS} = 25\text{V}$ $V_{GS} = 0$ $T_C = +125^\circ\text{C}$
6					500		
7	I _{D(ON)}	ON Drain Current ¹	0.3			A	$V_{DS} = 10\text{V}$, $V_{GS} = 10\text{V}$
8	r _{DS(ON)}	Drain-Source ON Resistance ¹		2.8	5.0	ohms	$V_{GS} = 10\text{V}$ $I_D = 200\text{mA}$ $T_C = +125^\circ\text{C}$
9					9.0		
10	g _{fs}	Common-Source Forward Transcond. ¹	100	300		mmhos	$V_{DS} = 10\text{V}$, $I_D = 0.2\text{A}$ $f = 1\text{KHz}$
11	C _{iss}	Common-Source Input Capacitance			60	pF	$V_{DS} = 25\text{V}$, $V_{GS} = 0$ $f = 1\text{MHz}$
12	C _{rss}	Common-Source Reverse Transfer Capacitance			5.0		
13	C _{oss}	Common-Source Output Capacitance			2.5		
14	t _{on}	Turn ON Time			10	nSec	$V_{DD} = 25\text{V}$, $V_{G(ON)} = 10\text{V}$ $R_L = 23\Omega$, $R_G = 51\Omega$
15	t _{off}	Turn OFF Time			10		

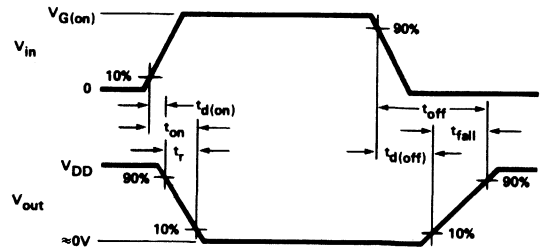
SWITCHING TIMES TEST CIRCUIT



INPUT PULSE
 $t_r < 0.5\text{ nSEC}$
 PULSE WIDTH - 100 nSEC

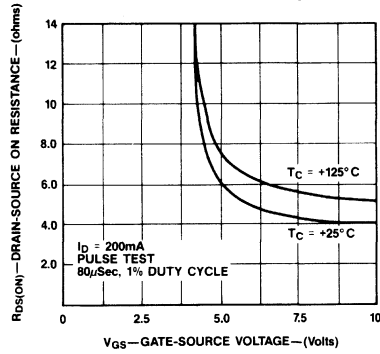
SAMPLING OSCILLOSCOPE
 $t_r < 0.38\text{ nSEC}$
 $R_{in} > 1\text{M}\Omega$
 $C_{in} < 2.0\text{ pF}$

TEST WAVEFORMS

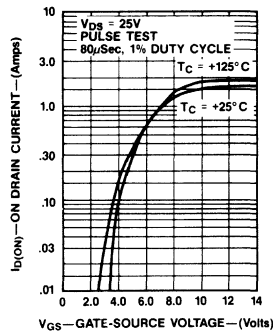


TYPICAL PERFORMANCE CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise specified)

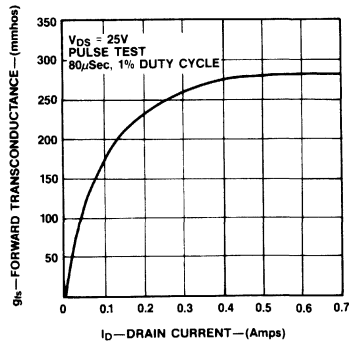
DRAIN-SOURCE ON RESISTANCE
—vs—
GATE-SOURCE VOLTAGE



ON DRAIN CURRENT
—vs—
GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE
—vs—
ON DRAIN CURRENT



N-CHANNEL ENHANCEMENT-MODE LATERAL D-MOS FETs

ORDERING INFORMATION



FEATURES

- High Gain—8.0dB min. @ 1GHz
- Low Noise—5.0dB max. @ 1GHz SD202, SD203
- Low Interelectrode Capacitances

APPLICATIONS

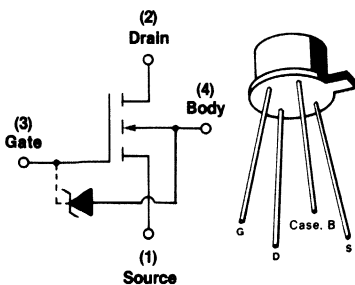
- High-Gain VHF/UHF Amplifiers, Oscillators, and Mixers

ABSOLUTE MAXIMUM RATINGS (T_A = +25 °C unless otherwise noted)

PARAMETER	SD200	SD201	SD202	SD203	UNIT
Breakdown Voltages					
V _{DS}	+25	+25	+20	+20	Vdc
V _{DB}	+25	+25	+20	+20	Vdc
V _{GS}	±40	-0.3	±40	-0.3	Vdc
		+20		+20	Vdc
V _{GB}	±40	-0.3	±40	-0.3	Vdc
		+20		+20	Vdc
V _{GD}	±40	-0.3	±40	+0.3	Vdc
		+20		+20	Vdc

I _D	Continuous Drain Current	50mA
P _T	Power Dissipation (at or below T _C = +25 °C)	1.8W
	Linear Derating Factor	18 mW/°C
P _D	Power Dissipation (at or below T _A = +25 °C)	360mW
	Linear Derating Factor	3.6 mW/°C
T _j	Operating Junction Temperature Range	-55 to +125 °C
T _s	Storage Temperature Range	-65 to +175 °C

SCHEMATIC DIAGRAM

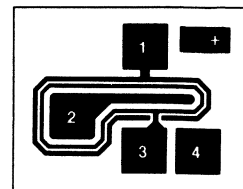


Body Internally connected to Case.
Diode protection on SD201/SD203 only.

PACKAGE DIMENSIONS TO-52, 4-LEAD

(See Package 2)

CHIP CONFIGURATION



PAD

- 1—Source
- 2—Drain
- 3—Gate
- 4—Diode

For SD201-203CHP bond Gate and Diode to common point. Body is backside contact. Dimensions: .022 x .025 x .013 inches

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	PARAMETER		SD200, SD201			SD202, SD203			UNIT	TEST CONDITIONS	
			MIN	TYP	MAX	MIN	TYP	MAX			
1	B _{VDS}	Drain-Source Breakdown Voltage	25	30		20	25		V	I _D = 1.0μA, V _{GS} = V _{BS} = 0	
2		Drain-Substrate Breakdown Voltage	25			20				I _D = 1.0μA, V _{GB} = 0 Source OPEN	
3	I _{D(off)}	Drain-Source OFF Current			1.0				μA	V _{DS} = 25V	V _{GS} = V _{BS} = 0
4							1.0			V _{DS} = 20V	
5	I _{GBS}	Gate-Body Leakage Current	SD200		±0.1				nA	V _{GB} = ±40V	V _{DB} = V _{SB} = 0
6			SD202					±0.1			
7			SD201		1.0				μA	V _{GB} = 20V	
8			SD203					1.0			
9	V _{GS(th)}	Gate Threshold Voltage	0.1	1.0	2.0	0.1	1.0	2.0	V	V _{DS} = V _{GS} , I _D = 1μA, V _{SB} = 0	
10	r _{DS(on)}	Drain-Source ON Resistance		40	70		35	50	ohms	V _{GS} = 5V I _D = 1mA V _{SB} = 0	
11	g _{fs}	Common-Source Forward Transcond.	13	14		17	20		mmhos	I _D = 20mA V _{DS} = 15V f = 1KHz, V _{SB} = 0	
12	c _{iss}	Common-Source Input Capacitance		2.4	3.0		3.0	3.6	pF	I _D = 20mA	V _{DS} = 15V f = 1MHz V _{SB} = 0
13	c _{oss}	Common-Source Output Capacitance		1.0	1.2		1.0	1.2		V _{GS} = 0	
14	c _{rss}	Common-Source Reverse Transfer Capacitance		0.2	0.3		0.2	0.3			
15	G _{ps}	Common-Source Power Gain	8.0	10		8.0	10			dB	
16	NF	Noise Figure		4.5	6.0		4.0	5.0	dB	I _D = 20mA	
17	P _i	Intercept Point		29			29		dBm	Δf = 2MHz	V _{SB} = 0

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION



FEATURES

- Low Capacitance— c_{iss} 11pF typ.
- Inherently Temperature Stable by Design
- TTL Logic Compatible Input— $V_{GS(th)}$ 2.0V (max)

APPLICATIONS

- Broadband RF Power Amplifiers
- High Speed Switches and Drivers
- Pulse Amplifiers and Logic Buffers
- CMOS and TTL to High Current Interface

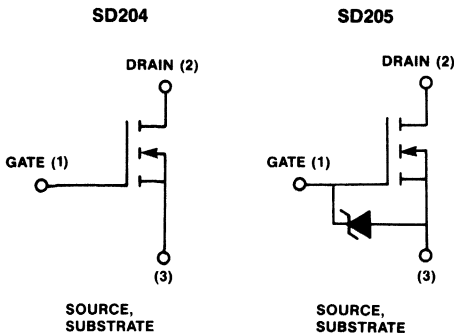
ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

V_{DS}	Drain-Source Voltage	+ 25V
V_{DG}	Drain-Gate Voltage	+ 25V
V_{GS}	Gate-Source (Forward) Voltage	+ 20V
	Gate-Source (Reverse) Voltage	-0.3V
I_D	Continuous Drain Current (Note 1)	0.3A
	Continuous Drain Current (Note 2)	0.7A
	Peak Pulsed Drain Current	1.0A
P_D	Continuous Power Dissipation		
	$T_A = +25^\circ\text{C}$ (Note 1, Note 3)	1.0W
	$T_C = +25^\circ\text{C}$ (Note 1, Note 4)	6.25W
	Power Derating Factors (Note 1)		
	Free Air	10mW/ $^\circ\text{C}$
	Infinite Heat Sink	62.5mW/ $^\circ\text{C}$

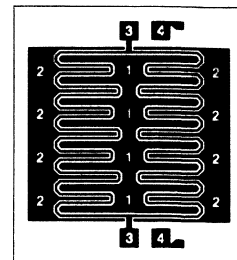
Thermal Resistance (Note 1)			
θ_{ja}	Junction to Ambient	100 $^\circ\text{C}/\text{W}$
θ_{jc}	Junction to Case	16 $^\circ\text{C}/\text{W}$
T_{op}	Operating Junction		
	Temperature Range	-55 to +125 $^\circ\text{C}$
T_{stg}	Storage Temperature Range	-55 to +150 $^\circ\text{C}$

- Note 1:** Not applicable to chips. Final value depends on mounting.
Note 2: Pulse Test 80 μSec , 1% Duty Cycle
Note 3: Free Air
Note 4: Infinite Heat Sink

SCHEMATIC DIAGRAM



CHIP CONFIGURATION



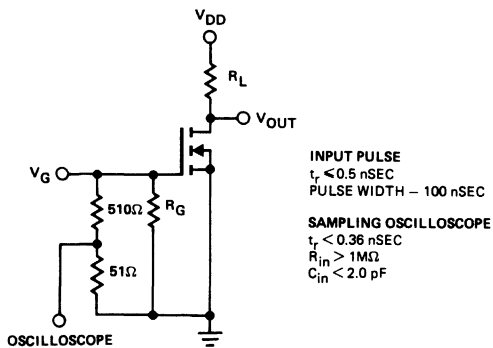
1—Drain 2—Source 3—Gate 4—Diode
 Minimum bonding required. One Drain, One Source (left), One Source (right), One Gate. Bond Gate and Adjacent Diode to Common Point to Connect Protective Diode.

Size: .040 x .044 x .013 inch.
 Body (Substrate) is backside contact.

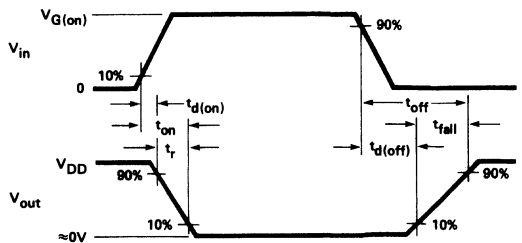
ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
1	BV_{DSS}	Drain Source Breakdown Voltage	25			V	$I_D = 1.0\mu\text{A}, V_{GS} = 0$	
2	$V_{GS(th)}$	Gate Source Threshold Voltage	0.5		2.0	V	$I_D = 1\text{mA}, V_{DS} = V_{GS}$	
3	STATIC	$I_{D(on)}$	1.0			nA	$V_{DS} = 10\text{V}$ (Note 1) $V_{GS} = 10\text{V}$	
4		I_{DSS}					1.0	$V_{DS} = 25\text{V}, V_{GS} = 0$
5		$r_{DS(on)}$	Drain-Source ON Resistance			ohms	$V_{GS} = 5\text{V}$	
6							$I_D = 50\text{mA}$ (Note 1)	
7	$V_{GS} = 10\text{V}$							
8	I_{GSS}	Gate Body Leakage Current	SD205		1.0	μA	$V_{GS} = 20\text{V}, V_{DS} = 0$	
8A			SD204		± 10	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0$	
9	g_{fs}	Common-Source Forward Transconductance	100			mmhos	$V_{DS} = 15\text{V}, I_D = 200\text{mA}$ $f = 1\text{KHz}$ (Note 1)	
10	C_{iss}	Common-Source Input Capacitance		11	13	pF	$V_{DS} = 10\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$	
11	C_{oss}	Common-Source Output Capacitance			8.0			
12	C_{rss}	Common-Source Reverse Transfer Capacitance			3.0			
13	$t_{d(on)}$	Turn-On Delay Time		<1.0	2.0			
14	DYNAMIC	t_r	Rise Time		1.0	3.0	nS	$V_{DD} = 10\text{V}, V_{G(on)} = 10\text{V}$ $R_L = 133\Omega, R_G = 51\Omega$
15		t_{off}	Turn-off Time		3.0	5.0		
16		NF	Common-Source Noise Figure			4.5		
17	G_{PS}	Common-Source Power Gain	9.0					

SWITCHING TIMES TEST CIRCUIT

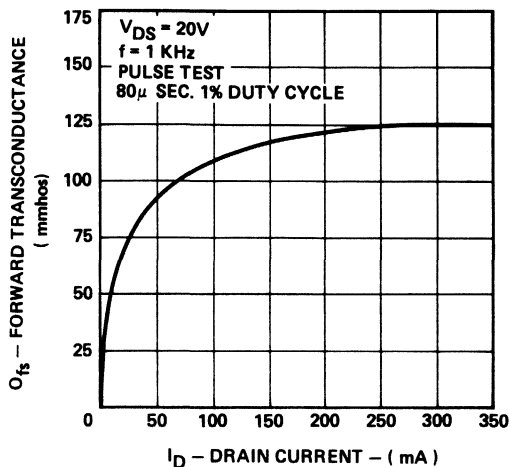


TEST WAVEFORMS

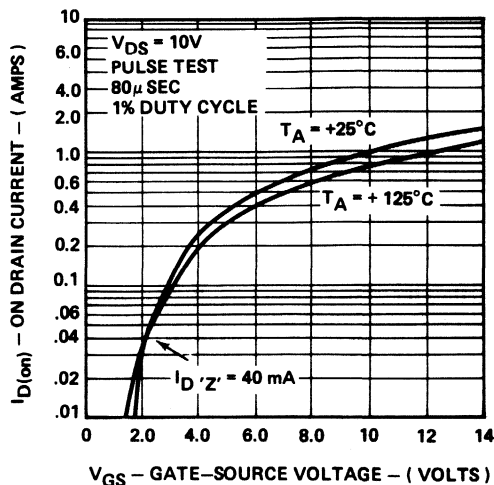


TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

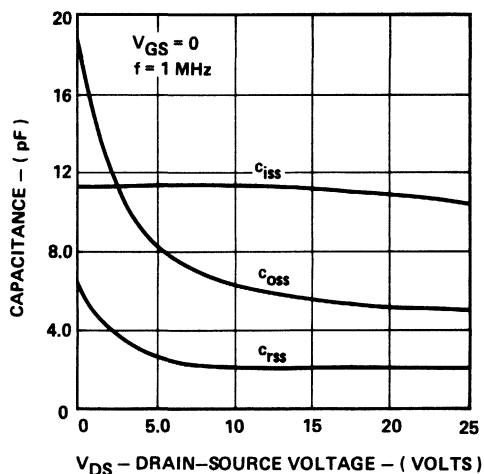
FORWARD TRANSCONDUCTANCE
—VS—
ON DRAIN CURRENT



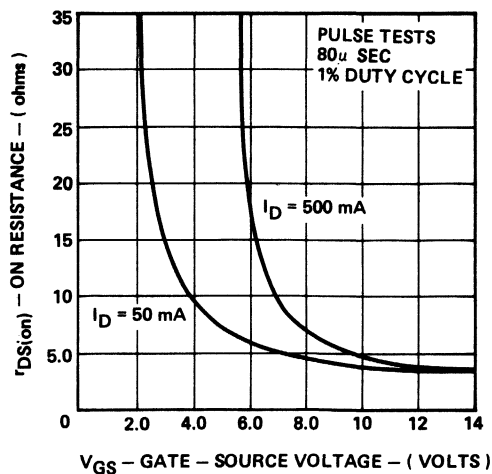
ON DRAIN CURRENT
—VS—
GATE-SOURCE VOLTAGE



CAPACITANCES
—VS—
DRAIN-SOURCE VOLTAGE



DRAIN-SOURCE ON RESISTANCE
—VS—
GATE-SOURCE VOLTAGE



N-CHANNEL ENHANCEMENT-MODE D-MOS FET SWITCHES

ORDERING INFORMATION

TO-206AF (TO-72) Package	SD210DE	SD211DE	SD212DE	SD213DE	SD214DE	SD215DE
Surface Mount	SD210DESR	SD211DESR	SD212DESR	SD213DESR	SD214DESR	SD215DESR
Chip Carrier in Carriers	SD210CHP	SD211CHP	SD212CHP	SD213CHP	SD214CHP	SD215CHP

FEATURES

- High Input to Output Isolation—120dB typical
- Low feedthrough and feedback transients
- Low Inter-electrode Capacitances

APPLICATIONS

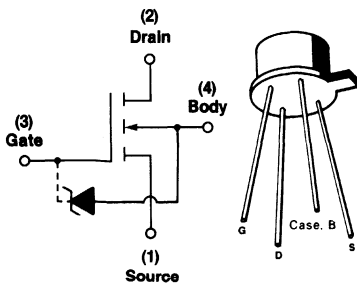
- +30V Switch Drivers—SD210, SD211
- ±10V Analog Switches—SD214, SD215
- ±5V Analog Switches—SD212, SD213

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

PARAMETER	SD210	SD211	SD212	SD213	SD214	SD215	UNIT
Breakdown Voltages							
V _{DS}	+30	+30	+10	+10	+20	+20	Vdc
V _{SD}	+10	+10	+10	+10	+20	+20	Vdc
V _{DB}	+30	+30	+15	+15	+25	+25	Vdc
V _{SB}	+15	+15	+15	+15	+25	+25	Vdc
V _{GS}	±40	-15	±40	-15	±40	-25	Vdc
		+25		+25		+30	Vdc
V _{GB}	±40	-0.3	±40	-0.3	±40	-0.3	Vdc
		+25		+25		+30	Vdc
V _{GD}	±40	-30	±40	-15	±40	-25	Vdc
		+25		+25		+30	Vdc

I _D	Continuous Drain Current	50mA
P _T	Power Dissipation (at or below T _C = +25°C)	1.2W
	Linear Derating Factor	12mW/°C
P _D	Power Dissipation (at or below T _A = +25°C)	300mW
	Linear Derating Factor	3.0mW/°C
T _J	Operating Junction Temperature Range	-55 to +125°C
T _S	Storage Temperature Range	-65 to +175°C

SCHEMATIC DIAGRAM



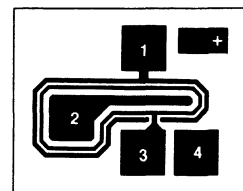
Body internally connected to Case.

Diode protection on SD211/SD213/SD215 only.

PACKAGE DIMENSIONS (TO-72) TO-206AF

(See Package 3)

CHIP CONFIGURATION



PAD
1—Source
2—Drain
3—Gate
4—Diode

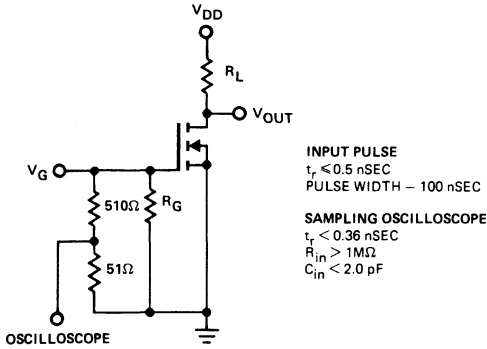
For SD211/213/215CHP bond Gate and Diode to common point. Body is backside contact.

Dimensions: .022 × .025 × .013 inches

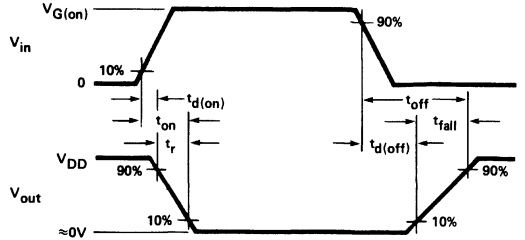
ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	PARAMETER		SD210, SD211			SD212, SD213			SD214, SD215			UNIT	TEST CONDITIONS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
1	BV _{DS}	Drain-Source Breakdown Voltage	30	35							V	I _D = 10 μ A V _{GS} = V _{BS} = 0	
2			10	25		10	25		20	25		V	I _D = 10nA V _{GS} = V _{BS} = -5V
3	BV _{SD}	Source-Drain Breakdown Voltage	10			10			20		V	I _S = 10nA V _{GD} = V _{BD} = -5V	
4	BV _{DB}	Drain-Substrate Breakdown Voltage	15			15			25		V	I _D = 10nA, V _{GB} = 0 Source OPEN	
5	BV _{SB}	Source-Substrate Breakdown Voltage	15			15			25		V	I _S = 10 μ A, V _{GB} = 0 Drain OPEN	
6	I _D (off)	Drain-Source OFF Current			10			10			nA	V _{DS} = 10V V _{GS} = V _{BS} = -5V	
7										10	nA	V _{DS} = 20V	
8	I _S (off)	Source-Drain OFF Current			10			10			nA	V _{SD} = 10V V _{GD} = V _{BD} = -5V	
9										10	nA	V _{SD} = 20V	
10	I _{GBS}	Gate-Body Leakage Current	SD210		0.1						nA	V _{GB} = \pm 40V V _{DB} = V _{SB} = 0	
11			SD212				0.1				nA		
12			SD214							0.1	nA		
13			SD211			10					μ A		
14			SD213					10			μ A		
15	SD215							10	μ A	V _{GB} = 30V			
16	V _{GS} (th)	Gate Threshold Voltage	0.5	1.0	2.0	0.1		2.0	0.1	1.0	2.0	V	V _{DS} = V _{GS} , I _D = 1 μ A, V _{SB} = 0
17	r _{DS} (on)	Drain-Source ON Resistance		50	70		50	70		50	70	ohms	V _{GS} = 5V I _D = 1mA
18				30	45		30	45		30	45	ohms	V _{GS} = 10V V _{SB} = 0
19	g _{fs}	Common-Source Forward Transcond.	10	12		10	12		10	12		mmhos	V _{DS} = 10V, I _D = 20mA f = 1kHz, V _{SB} = 0
20	C _(gs + gd + gb)	Gate Node Capacitance		2.4	3.5		2.4	3.5		2.4	3.5	pF	V _{DS} = 10V V _{GS} = V _{BS} = -15V f = 1MHz
21	C _(gd + db)	Drain Node Capacitance		1.3	1.5		1.3	1.5		1.3	1.5	pF	
22	C _(gs + sb)	Source Node Capacitance		3.5	4.0		3.5	4.0		3.5	4.0	pF	
23	C _(dg)	Reverse Transfer Capacitance		0.3	0.5		0.3	0.5		0.3	0.5	pF	
24	t _{d(on)}	Turn ON Delay Time		0.7	1.0		0.7	1.0		0.7	1.0	nSec	V _{DD} = 5V, V _{G(on)} = 10V R _L = 680 Ω , R _G = 51 Ω
25	t _r	Rise Time		0.8	1.0		0.8	1.0		0.8	1.0		
26	t _{off}	Turn OFF Time		10			10			10			

SWITCHING TIMES TEST CIRCUIT

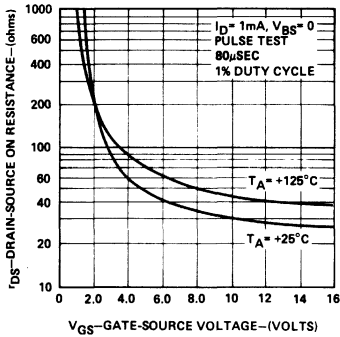


TEST WAVEFORMS

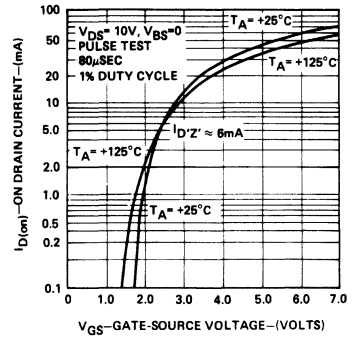


TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

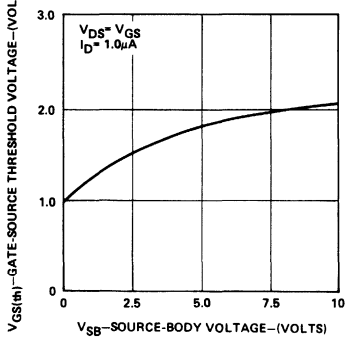
DRAIN-SOURCE ON RESISTANCE
—vs—
GATE-SOURCE VOLTAGE



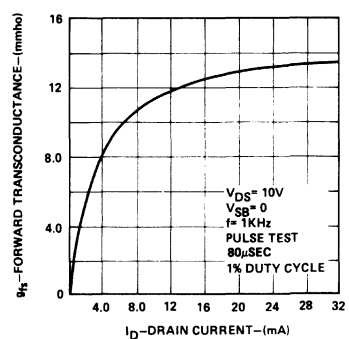
ON DRAIN CURRENT
—vs—
GATE-SOURCE VOLTAGE



GATE-SOURCE THRESHOLD VOLTAGE
—vs—
SOURCE-BODY VOLTAGE



FORWARD TRANSCONDUCTANCE
—vs—
ON DRAIN CURRENT



N-CHANNEL ENHANCEMENT-MODE D-MOS FET SWITCHES

ORDERING INFORMATION



FEATURES

- ◆ High Input to Output Isolation — 120dB typical
- ◆ Low feedthrough and feedback transients
- ◆ Low Inter-electrode Capacitances
- ◆ Low Gamma Process
- ◆ On Resistance Guaranteed In Analog Switch Configuration

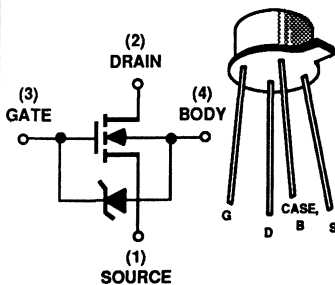
APPLICATIONS

- ◆ +30V Switch Driver — SD211A
- ◆ ±10V Analog Switch — SD215A
- ◆ ±5V Analog Switch — SD211A

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

PARAMETER	SD211A	SD215A	UNIT		
Breakdown Voltages				I _D	Continuous Drain Current 50mA
V _{DS}	+30	+20	V	P _T	Power Dissipation (@ or below T _C = +25°C) 1.2W
V _{SD}	+10	+20	V		Linear Derating Factor 12mW/°C
V _{DB}	+30	+25	V	P _D	Power Dissipation (@ or below T _A = +25°C) 300mW
V _{SB}	+15	+25	V		Linear Derating Factor 3.0mW/°C
V _{GS}	-15	-25	V	T _j	Operating Junction Temperature Range -55°C to +125°C
	+25	+30	V	T _s	Storage Temperature Range -65°C to +175°C
V _{GB}	-0.3	-0.3	V		
	+25	+30	V		
V _{GD}	-30	-25	V		
	+25	+30	V		

SCHEMATIC DIAGRAM

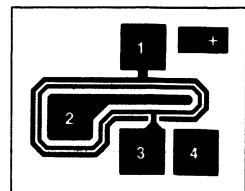


Body Internally connected to Case.

PACKAGE DIMENSIONS (TO-72) TO-206AF

(See Package 3)

CHIP CONFIGURATION



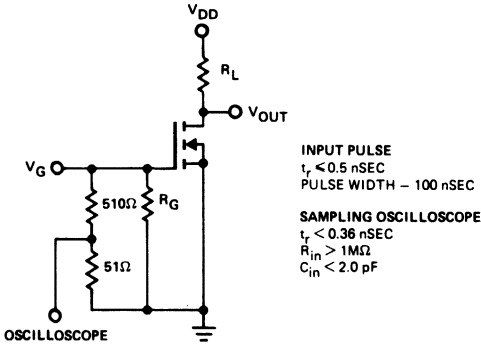
PAD
1 - Source
2 - Drain
3 - Gate
4 - Diode

Dimensions: 0.022 x 0.025 x 0.013 inches

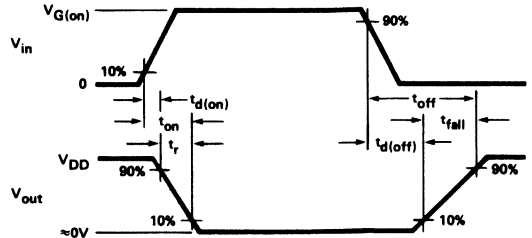
ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	PARAMETER		SD211A			SD215A			UNIT	TEST CONDITIONS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
1	S T A T I C	BV _{DS}	30	35					V	I _D = 10 μ A, V _{GS} = V _{BS} = 0
2		Drain-Source Breakdown Voltage	10	25		20	25		V	I _D = 10nA, V _{GS} = V _{BS} = -5V
3		BV _{SD}	10			20			V	I _S = 10nA, V _{GD} = V _{BD} = -5V
4		BV _{DB}	15			25			V	I _D = 10nA, V _{GB} = 0 Source OPEN
5		BV _{SB}	15			25			V	I _S = 10 μ A, V _{GB} = 0 Drain OPEN
6	S T A T I C	I _{D(off)}			10				nA	V _{DS} = 10V
7		Drain-Source Off Current						10	nA	V _{DS} = 20V
8		I _{S(off)}			10				nA	V _{SD} = 10V
9		Source-Drain Off Current						10	nA	V _{SD} = 20V
10	S T A T I C	I _{GBS}			10				μ A	V _{GB} = 25V
11		Gate-Body Leakage Current						10	μ A	V _{GB} = 30V
12		V _{GS(th)}	0.75	1.0	1.5	0.75	1.0	1.5	V	V _{DS} = V _{GS} , I _D = 1.0 μ A V _{SB} = 0
13	S T A T I C	r _{DS(on)}	Drain-Source On Resistance			90			ohms	V _{GS} = 4.5V, I _D = 1mA V _{SB} = 5V
14								90		V _{GS} = 4.5V, I _D = 1mA V _{SB} = 10V
15					30	45		30		45
16	D Y N A M I C	g _{fs}	10	13		10	13		mmhos	V _{DS} = 10V, I _D = 20mA f = 1kHz, V _{SB} = 0
17		C _(gs+gd+gb)		2.4	3.5		2.4	3.5	pF	V _{DS} = 10V, V _{GS} = V _{BS} = -15V,
18		C _(gd+db)		1.3	1.5		1.3	1.5	pF	f = 1MHz
19		C _(gs+sb)		3.5	4.0		3.5	4.0	pF	
20		C _(dg)		0.3	0.5		0.3	0.5	pF	
21		t _{D(on)}	Turn ON Delay Time	0.7	1.0		0.7	1.0		nsec
22	t _r	Rise Time	0.8	1.0		0.8	1.0			
23	t _{off}	Turn OFF Time	10			10				

SWITCHING TIMES TEST CIRCUIT

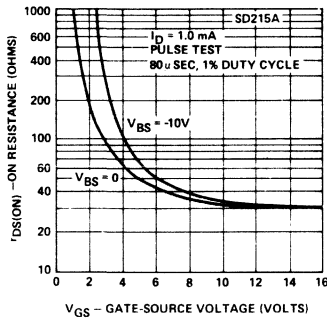


TEST WAVEFORMS

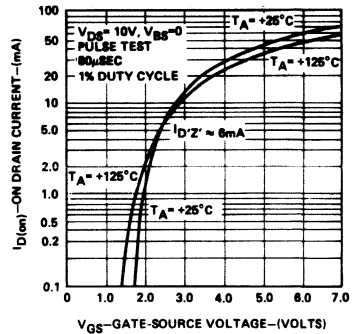


TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

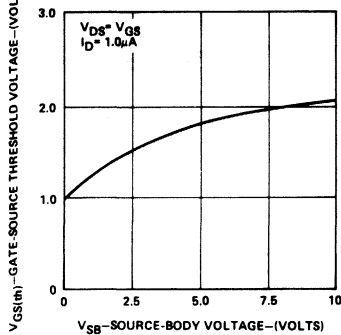
DRAIN-SOURCE ON RESISTANCE
—vs—
GATE-SOURCE VOLTAGE



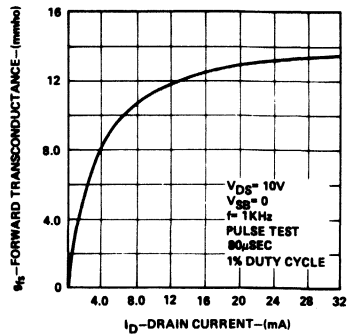
ON DRAIN CURRENT
—vs—
GATE-SOURCE VOLTAGE



GATE-SOURCE THRESHOLD VOLTAGE
—vs—
SOURCE-BODY VOLTAGE



FORWARD TRANSCONDUCTANCE
—vs—
ON DRAIN CURRENT



N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FET

ORDERING INFORMATION

TO-206AF TO-206AF	SD217DE	SD219DE
TO-206AF TO-206AF	SD217DE	SD219DE
TO-206AF TO-206AF	SD217DE	SD219DE
Description / V _{GS} / V _{DS}	5.0 ohm, 20V V _{GS} = 15V min	5.0 ohm, 20V V _{GS} = 20V min

FEATURES

- CMOS Compatible Input
- Small Package, Standard Pin-Out
- TTL and CMOS Compatible Input
- Low Capacitance
- Peak Pulsed Current, 1 Amp min

APPLICATIONS

- ± 10V Analog Switch, SD219DE
- ± 7.5 Analog Switch, SD217DE
- High Speed, Medium Power, Switch Drivers
- Sample and Hold and Track and Hold
- A-to-D and D-to-A Converters

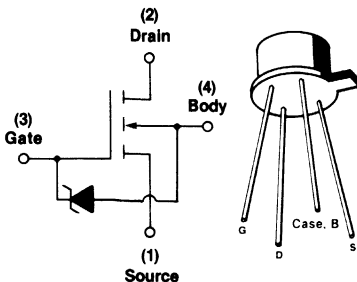
ABSOLUTE MAXIMUM RATINGS (T_A = + 25 °C unless otherwise specified)

V _{DS} Drain-Source Voltage	+ 25V
V _{DB} Drain-Body Voltage	
SD217	+ 22.5V
SD219	+ 25V
V _{SD} Source-Drain Voltage	
SD217	+ 15V
SD219	+ 20V
V _{SB} Source-Body Voltage	
SD217	+ 22.5V
SD219	+ 25V
V _{GB} Gate-Body Voltage	+ 30V
V _{GS} Gate-Source Voltage	± 22.5V
V _{GD} Gate-Drain Voltage	± 22.5V
I _D Peak Pulsed Drain Current	+ 1.0A

I _D Continuous Drain Current (Note 1)	160mA
P _D Continuous Power Dissipation (Note 1)	
T _A = + 25 °C (Free Air)	300mW
T _C = + 25 °C (Infinite Heat Sink)	1.2W
Power Derating Factors (Note 1)	
Free Air	3.0mW/°C
Infinite Heat Sink	12mW/°C
Thermal Resistance (Note 1)	
O _{ja} Junction to Ambient	333 °C/W
O _{jc} Junction to Case	83 °C/W
T _{op} Operating Junction	
Temperature Range	-55 to + 125 °C
T _{stg} Storage Temperature Range	-55 to + 150 °C

Note 1: Not applicable to chips. Final value depends on mounting.

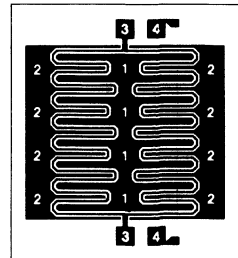
SCHEMATIC DIAGRAM



PACKAGE DIMENSIONS (TO-72) TO-206AF

(See Package 3)

CHIP CONFIGURATION



1—Drain 2—Source 3—Gate 4—Diode
Minimum bonding required. One Drain, One Source (left), One Source (right), One Gate. Bond Gate and Adjacent Diode to Common Point to Connect Protective Diode.

Size: .040 x .044 x .013 inch.

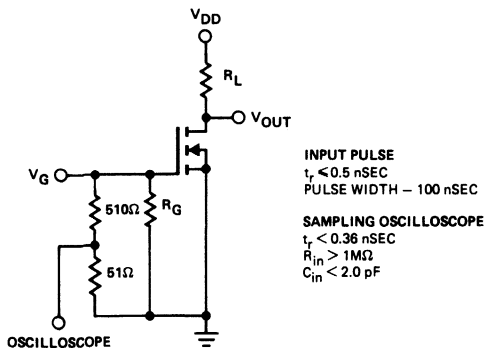
Body (Substrate) is backside contact.

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

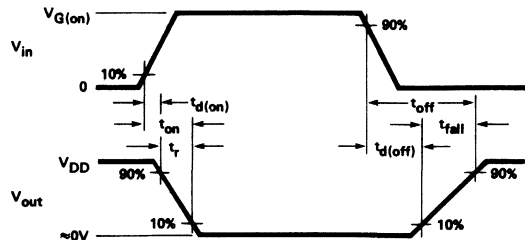
#	CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
1	BV _{DS}	Drain-Source Breakdown Voltage	25	30		V	I _D = 10μA, V _{GS} = V _{BS} = 0	
2			15	20			I _D = 100nA, V _{GS} = V _{BS} = -5V	
3	BV _{SD}	Source-Drain Breakdown Voltage	SD217	15		V	I _S = 100nA, V _{GD} = V _{BD} = -5V	
4			SD219	20				
5	BV _{DB}	Drain-Body Breakdown Voltage	SD217	22.5		V	I _D = 100nA, V _{GB} = 0, Source Open	
6			SD219	25				
7	BV _{SB}	Source-Body Breakdown Voltage	SD217	22.5		V	I _S = 100nA, V _{GB} = 0, Drain Open	
8			SD219	25				
9	I _{D(off)}	Drain-Source OFF Leakage Current			100	nA	V _{DS} = 15V, V _{GS} = V _{BS} = -5V	
10		Source-Drain OFF Leakage Current			100		V _{SD} = 15V, V _{GD} = V _{BD} = -5V	
11	I _{GB}	Gate-Body ON Leakage Current			10	μA	V _{GB} = 30V, V _{GS} = V _{GD} = 22.5V	
12	V _{GS(th)}	Gate-Source Threshold Voltage	0.1		2.0	V	V _{DS} = V _{GS} , I _D = 10μA, V _{SB} = 0	
13	I _{D(on)}	Drain-Source ON Current (Note 1)	1.0			A	V _{DS} = V _{GS} = 10V, V _{SB} = 0	
14	r _{DS(on)}	Drain-Source ON Resistance (Note 1)			8.0	ohms	V _{GS} = 5.0V	I _D = 50mA V _{SB} = 0
15					6.0		V _{GS} = 10V	I _D = 500mA V _{SB} = 0
16					6.0			
17	g _{fs}	Common-Source (Note 1) Forward Transconductance	100			mmhos	V _{DS} = 15V, I _D = 200mA V _{SB} = 0, F = 1KHz	
18	C _(gs + gd + gb)	Gate Node Capacitance			30	pF	V _{DS} = 10V, V _{GS} V _{BS} = -15V f = 1MHz	
19		Drain-Node Capacitance			15			
20		Source Node Capacitance			40			
21		Reverse Transfer Capacitance			5.0			
22		t _{on}	Turn ON Time		2.0			
23	t _{off}	Turn OFF Time		3.0	5.0			

Note 1: Pulse Test 80μSec, 1% Duty Cycle

SWITCHING TIMES TEST CIRCUIT

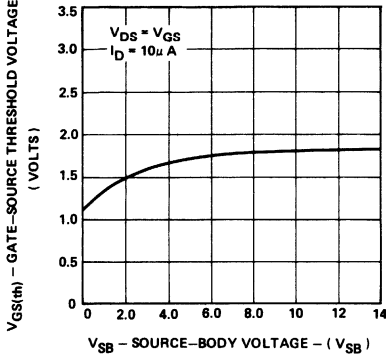


TEST WAVEFORMS

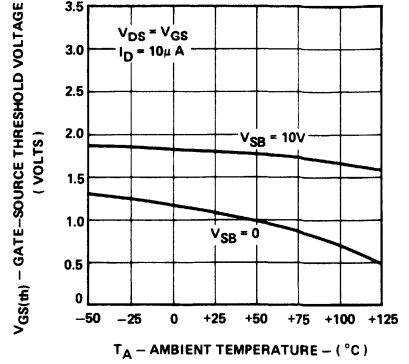


TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

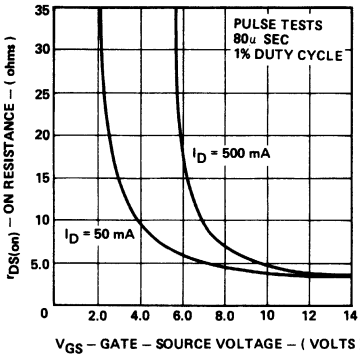
GATE-SOURCE THRESHOLD VOLTAGE
—VS—
SOURCE-BODY VOLTAGE



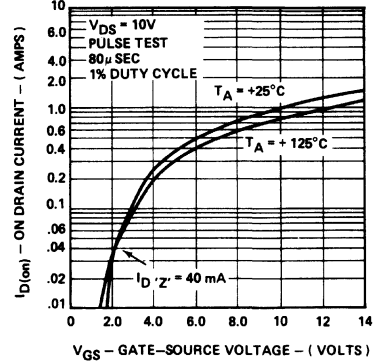
GATE-SOURCE THRESHOLD VOLTAGE
—VS—
TEMPERATURE



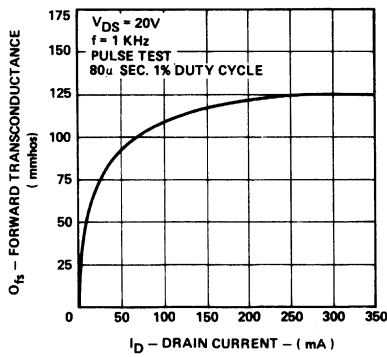
DRAIN-SOURCE ON RESISTANCE
—VS—
GATE-SOURCE VOLTAGE



ON DRAIN CURRENT
—VS—
GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE
—VS—
ON DRAIN CURRENT



N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FET

ORDERING INFORMATION



FEATURES

- Low Capacitance - c_{iss} 12pF, c_{rss} 0.6pF - (typ)
- Fast Switching
- TTL Logic Compatible Input $V_{GS(th)}$ 2.3V (max.)

APPLICATIONS

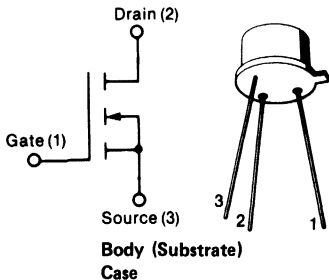
- Broadband RF Power Amplifiers
- High Speed Switch Drivers
- High Speed Display Drivers
- CMOS and TTL to High Current Interfaces

ABSOLUTE MAXIMUM RATINGS ($T_C = +25^\circ\text{C}$ unless otherwise noted)

V_{DS}	Drain-Source Voltage		
	SD220	+60V	
	SD221	+100V	
V_{DG}	Drain-Gate Voltage (RGS = 1M Ω)		
	SD220	+60V	
	SD221	+100V	
$V_{GS(F)}$	Gate-Source (Forward) Voltage ..	+30V	
$V_{GS(R)}$	Gate-Source (Reverse) Voltage ..	-30V	
I_D	Continuous Drain Current		
		$T_C = +100^\circ\text{C}$	$T_C = +25^\circ\text{C}$
	SD220HD	.32A	.51A
	SD221HD	.30A	.47A
I_{DM}	Peak Pulsed Drain Current		
	SD220	0.8A	
	SD221	0.6A	

P_D	Maximum Power Dissipation		
		$T_C = +100^\circ\text{C}$	$T_C = +25^\circ\text{C}$
	HD, TO-205AF Package	2.5W	6.25W
	Linear Derating Factor		
		Junction to Ambient (mW/ $^\circ\text{C}$)	Junction to Case (mW/ $^\circ\text{C}$)
	HD, TO-205AF Package	8.0	50
	Operating Junction and Storage Temperature Range	-55 $^\circ$ to +150 $^\circ\text{C}$	

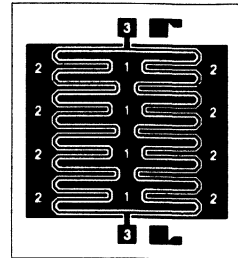
SCHEMATIC DIAGRAM



PACKAGE DIMENSIONS TO-205AF (TO-39)

(See Package 6)

CHIP CONFIGURATION



1—Drain 2—Source 3—Gate
Minimum bonding required. One Drain, One Source (left), One Source (right), One Gate.

Size: .040 x .044 x .013 inch.
Body (Substrate) is backside contact.

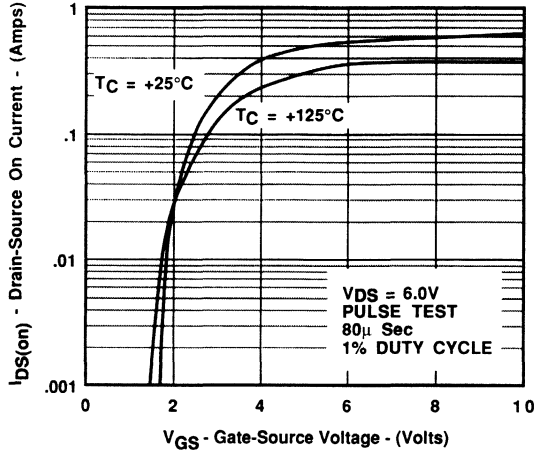
ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	Characteristic		SD220			SD221			Units	Test Conditions		
			Min	Typ	Max	Min	Typ	Max				
1	STATIC	BV _{DSS} Drain-Source Breakdown Voltage	60	80		100	115		V	I _D = 10 μ A, V _{GS} = 0		
2		V _{GS(th)} Gate-Source Threshold Voltage	0.1	0.8	2.3	0.1		2.3		I _D = 10 μ A, V _{DS} = V _{GS}		
3			0.5	1.5	3.0	0.5		3.0		I _D = 1mA, V _{DS} = V _{GS}		
4		I _{GSS} Gate Leakage Currents			± 10			± 10	nA	V _{GS} = ± 20 , V _{DS} = 0		
5	STATIC	I _{DSS} Drain-Source OFF Leakage Current		0.1	10				μ A	V _{DS} = 60V	V _{GS} = 0	
6							0.1	10		V _{DS} = 100V		
7					1.0				mA	V _{DS} = 48V	V _{GS} = 0	
8							1.0			V _{DS} = 80V	T _A = +125 $^\circ$ C	
9			I _{D(on)} ON (Note 1) Drain Current	500			300			V _{DS} = 6V	V _{GS} = 10V	
10				600	700		400			V _{DS} = 10V		
11			r _{DS(on)} Drain-Source ON Resistance (Note 1)		7.5	10			12	ohms	V _{GS} = 5V	
12						16			19.2		I _D = 50mA	T _A = +125 $^\circ$ C
13					6.5	9.0			10		V _{GS} = 10V	
14						15			16		I _D = 50mA	T _A = +125 $^\circ$ C
15								14	V _{GS} = 10V			
16								21	I _D = 250mA		T _A = +125 $^\circ$ C	
17				9.0	12				V _{GS} = 10V			
18				18				I _D = 500mA	T _A = +125 $^\circ$ C			
19	DYNAMIC	g _{fs} Common-Source Forward Transconductance (Note 1)	150	190		100			mmhos	V _{DS} = 30V, I _D = 300mA f = 1KHz (Note 1)		
20		c _{iss} Common-Source Input Capacitance		12	15		11	15	pF	V _{DS} = 30V, V _{GS} = 0 f = 1MHz		
21		c _{oss} Common-Source Output Capacitance		2.8	3.5		2.6	15				
22		c _{rss} Common-Source Reverse Transfer Capacitance		0.6	1.0		0.6	1.0				
23		t _{d(on)} Turn-On Delay Time		1.0	2.0		1.0	2.0				
24		t _r Rise Time		1.0	3.0		1.0	3.0	nS	V _{DD} = 30V V _{G(on)} = 5.0V R _L = 90 ohms R _G = 51 ohms		
25	t _f Fall Time		3.0	5.0		3.0	5.0					

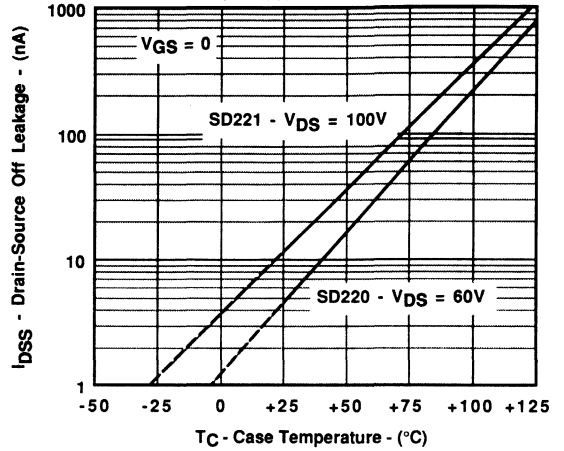
Note 1: Pulse Test 80 μ Sec, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise noted)

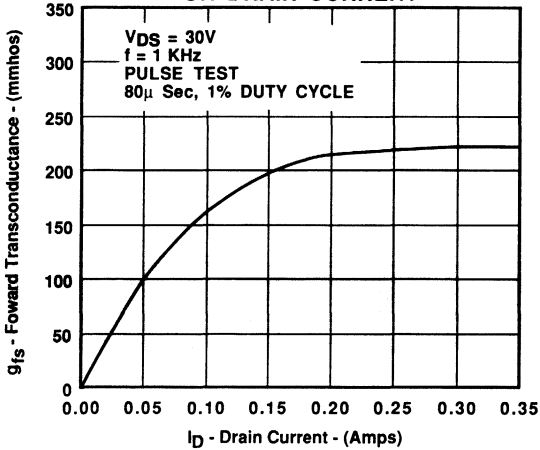
DRAIN-SOURCE ON CURRENT
-vs-
GATE-SOURCE VOLTAGE



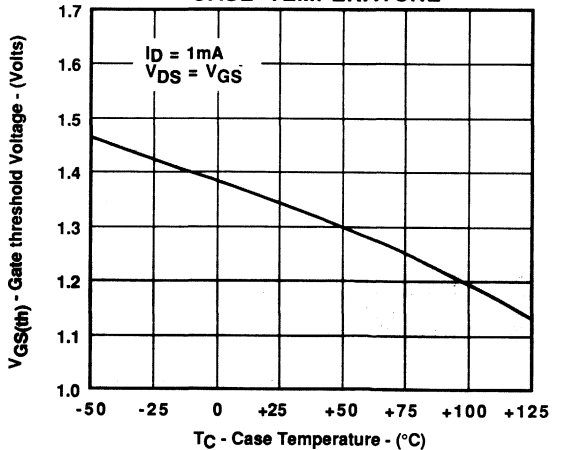
DRAIN-SOURCE OFF LEAKAGE
-vs-
CASE TEMPERATURE



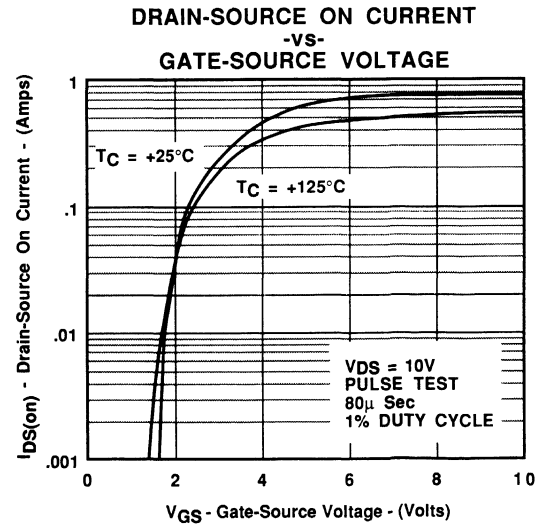
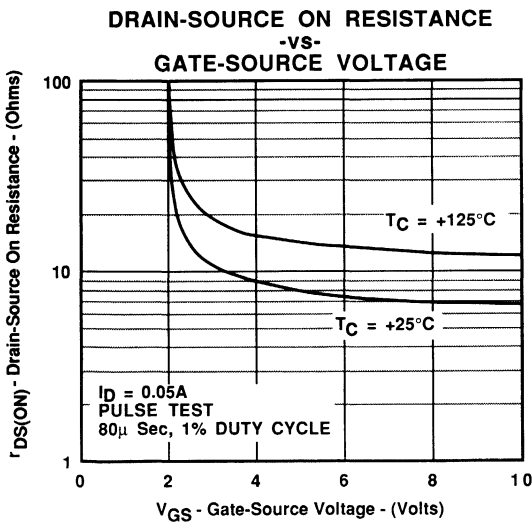
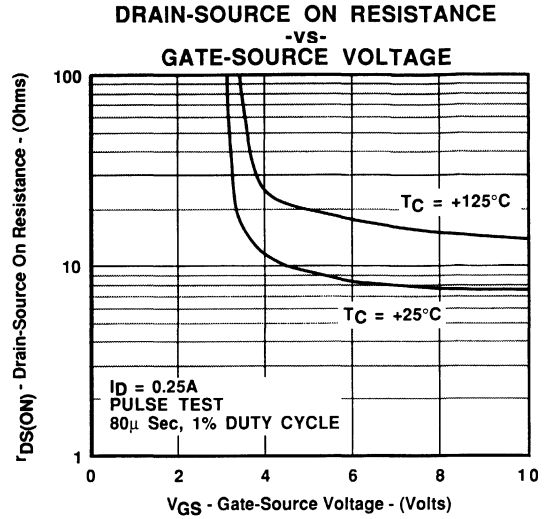
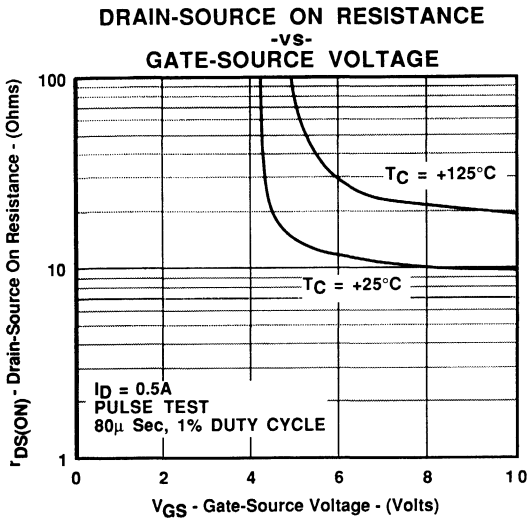
FORWARD TRANSCONDUCTANCE
-vs-
ON DRAIN CURRENT



GATE THRESHOLD VOLTAGE
-vs-
CASE TEMPERATURE



TYPICAL PERFORMANCE CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise noted)



N-CHANNEL ENHANCEMENT-MODE DUAL GATE D-MOS FET

ORDERING INFORMATION



FEATURES

- Normally Off-Enhancement-Mode Operation
- Dual Gate with Gate Protective Diodes
- Low Feedback Capacitance — C_{rss} .02pF (typ)
- Wide Dynamic Range-Remote AGC capability
- High Power Gain- 10dB min. @ 1GHz
- Low Noise-7.0dB max. @ 1GHz
- Low Cross-Modulation Distortion

APPLICATIONS

- Wide Band (Unneutralized) VHF/UHF Amplifiers
- VHF/UHF Linear Mixers

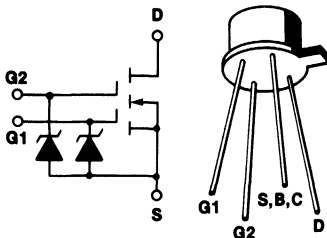
ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DS}	Drain-Source Voltage	+20V
V_{G1B}	Gate 1-Substrate Voltage	-0.3 to +10V
V_{G2B}	Gate 2-Substrate Voltage	-0.3 to +15V
I_D	Continuous Drain Current (Note 1)	50mA
P_D	Continuous Power Dissipation (Note 1)		
	$T_A = +25^\circ\text{C}$ (Free Air)	360mW
	$T_C = +25^\circ\text{C}$ (Infinite Heat Sink)	1.8W
	Power Derating Factors (Note 1)		
	Free Air	3.6mW/°C
	Infinite Heat Sink	18mW/°C

T_{op}	Operating Junction Temperature Range	-55 to +125°C
T_{stg}	Storage Temperature Range	..	-65 to +175°C

Note 1: Not applicable to chips. Final value depends mounting substrate.

SCHEMATIC DIAGRAM

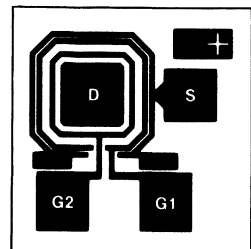


Pin 1-Drain, 2-Gate 2
Pin 3-Gate 1,
Pin 4-Source, Substrate, Case

PACKAGE DIMENSIONS

TO-52, 4-LEAD
(See Package 2)

CHIP CONFIGURATION



Chip backside connected to source
Dimensions: .022 x .022 x .013 inches

ELECTRICAL CHARACTERISTICS (TA = +25 °C unless otherwise noted)

#	PARAMETER		SD303			UNIT	TEST CONDITIONS	
			MIN	TYP	MAX			
1	BV _{DS}	Drain-Source Breakdown Voltage	20	25		V	I _D = 5μA V _{G1S} = V _{G2S} = 0	
2	I _{DSS}	Drain-Source OFF Leakage Current		.01	1.0	μA	V _{DS} = 15V V _{G1S} = V _{G2S} = 0	
3	I _{G1SS}	Gate 1 Leakage Current		1.0	100	nA	V _{G1S} = 5V V _{G2S} = V _{DS} = 0	
4	I _{G2SS}	Gate 2 Leakage Current		1.0	100	nA	V _{G2S} = 10V V _{G1S} = V _{DS} = 0	
5	V _{T1}	Gate 1-Source Threshold Voltage	0.1	0.5	1.5	V	V _{DS} = V _{G1S} V _{G2S} = 10V, I _D = 1μA	
6	V _{T2}	Gate 2-Source Threshold Voltage	0.1	0.5	1.5	V	V _{G1S} = 4V	V _{DS} = V _{G2S} I _D = 1μA
7	r _{DS(on)}	Drain-Source ON Resistance		65	80	ohms	I _D = 1mA, V _{G1S} = 5V V _{G2S} = 10V	
8	g _{fs}	Common-Source Forward Transconductance	13	15		mmhos	V _{DS} = 15V, I _D = 18mA V _{G2S} = 10V, f = 1KHz	
9	C _{iss}	Common-Source Input Capacitance		3.0	3.5	pF	V _{DS} = 15V, I _D = 18mA V _{G2S} = 10V, f = 1MHz	
10	C _{oss}	Common-Source Output Capacitance		0.6		pF	V _{DS} = 15V, V _{G1S} = 0 V _{G2S} = 10V, f = MHz	
11	C _{rss}	Common-Source Reverse Transfer Capacitance		.02		pF		
12	G _{ps}	Power Gain	10	14		dB	f = 1GHz	V _{DS} = 15V V _{G2S} = 10V I _D = 18mA
13	NF	Noise Figure		5.5	7.0	dB	f = 1GHz	
14	AGC (V _{G2S})	Range of Automatic Gain Control		40		dB	V _{G1S} ≅ 2.5V f = 500MHz	V _{DS} = 15V V _{G2S} = 10V to 0V
15	E _{INT}	Interfering Signal at Gate for 1% Cross-Modulation Distortion (Peak Voltage ref. to 300 ohm system)		150		mV	f _o = 1.000GHz f _i = 0.995GHz	V _{DS} = 15V V _{G2S} = 10V I _D = 18mA

N-CHANNEL ENHANCEMENT-MODE DUAL GATE D-MOS FET

ORDERING INFORMATION



FEATURES

- Normally Off-Enhancement-Mode Operation
- Dual Gate with Gate Protective Diodes
- Low Feedback Capacitance — C_{rss} .03pF (typ)
- Wide Dynamic Range-Remote AGC capability
- High Power Gain- 17dB min. @ 500MHz (SD306)
- Low Noise-8.0dB max. @ 500MHz (SD306)
- Low Cross-Modulation Distortion

APPLICATIONS

- Wide Band (Unneutralized) VHF/UHF Amplifiers
- VHF/UHF Linear Mixers

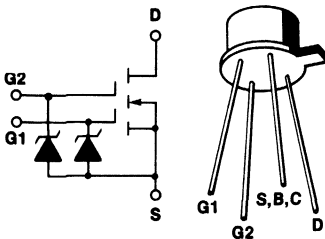
ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DS}	Drain-Source Voltage	
	SD304	+25V
	SD306	+20V
V_{G1B}	Gate 1-Substrate Voltage	
	SD304	-0.3 to +10V
	SD306	-0.3 to +20V
V_{G2B}	Gate 2-Substrate Voltage	
	SD304	-0.3 to +15V
	SD306	-0.3 to +20V
I_D	Continuous Drain Current (Note 1)	50mA

P_D	Continuous Power Dissipation (Note 1)	
	$T_A = +25^\circ\text{C}$ (Free Air)	300mW
	$T_C = +25^\circ\text{C}$ (Infinite Heat Sink)	1.2W
	Power Derating Factors (Note 1)	
	Free Air	3.0mW/ $^\circ\text{C}$
	Infinite Heat Sink	12mW/ $^\circ\text{C}$
T_{op}	Operating Junction Temperature Range	-55 to +125 $^\circ\text{C}$
T_{stg}	Storage Temperature Range ..	-65 to +175 $^\circ\text{C}$

Note 1: Not applicable to chips. Final value depends mounting substrate.

SCHEMATIC DIAGRAM

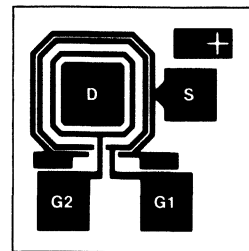


Pin 1-Drain, 2-Gate 2
Pin 3-Gate 1,
Pin 4-Source, Substrate, Case

PACKAGE DIMENSIONS (TO-72) TO-206AF

(See Package 3)

CHIP CONFIGURATION



Chip backside connected to source
Dimensions: .022 x .022 x .013 inches

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	PARAMETER		SD304			SD306			UNIT	TEST CONDITIONS
			MIN	TYP	MAX	MIN	TYP	MAX		
1	STATIC	BV_{DS} Drain-Source Breakdown Voltage	25	30		20	25		V	$I_D = 5\mu\text{A}$ $V_{G1S} = V_{G2S} = 0$
2		I_{DSS} Drain-Source OFF Leakage Current		.01	1.0		.01	1.0	μA	$V_{DS} = 15\text{V}$ $V_{G1S} = V_{G2S} = 0$
3		I_{G1SS} Gate 1 Leakage Current		1.0	100		1.0	100	nA	$V_{G1S} = 5\text{V}$ $V_{G2S} = V_{DS} = 0$
4		I_{G2SS} Gate 2 Leakage Current		1.0	100		1.0	100	nA	$V_{G2S} = 10\text{V}$ $V_{G1S} = V_{DS} = 0$
5		V_{T1} Gate 1-Source Threshold Voltage	0.1	1.0	2.0	0.1	0.5	1.5	V	$V_{DS} = V_{G1S}$ $V_{G2S} = 10\text{V}, I_D = 1\mu\text{A}$
6		V_{T2} Gate 2-Source Threshold Voltage	0.1	1.0	2.0				V	$V_{G1S} = 4\text{V}$ $V_{DS} = V_{G2S}$ $I_D = 1\mu\text{A}$
7						0.1	0.5	1.5	V	$V_{G1S} = 5\text{V}$
8		$r_{DS(on)}$ Drain-Source ON Resistance		90	130		65	100	ohms	$I_D = 1\text{mA}, V_{G1S} = 5\text{V}$ $V_{G2S} = 10\text{V}$
9	DYNAMIC	g_{fs} Common-Source Forward Transconductance	8.0	10		13	15		mmhos	$V_{DS} = 15\text{V}, I_D = 18\text{mA}$ $V_{G2S} = 10\text{V}, f = 1\text{KHz}$
10		C_{iss} Common-Source Input Capacitance		2.5	3.0		3.3	3.6	pF	$V_{DS} = 15\text{V}, I_D = 18\text{mA}$ $V_{G2S} = 10\text{V}, f = 1\text{MHz}$
11		C_{oss} Common-Source Output Capacitance		1.0	1.2		1.0	1.3		$V_{DS} = 15\text{V}, V_{G1S} = 0$ $V_{G2S} = 10\text{V}, f = 1\text{MHz}$
12		C_{rss} Common-Source Reverse Transfer Capacitance		.03			.03			
13		$Re(Y_{11})$ Input Admittance					1.11		mmhos	$V_{DS} = 15\text{V}, I_D = 18\text{mA}$
14	$Im(Y_{11})$					4.76		mmhos	$V_{G2S} = 10\text{V}, f = 200\text{MHz}$	

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SD304			SD306			UNIT	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX			
Re (Y22)	Output Admittance					1.05		mmhos	$V_{DS} = 15V, I_D = 18mA$ $V_{G2S} = 10V, f = 200MHz$	
Im (Y22)						1.54				
Re (Y21)	Forward Transmittance					13.23				
Im (Y21)						-5.62				
Re (Y12)	Reverse Transmittance					0.01				
Im (Y12)						-0.04				
G_{ps}	Power Gain	13	16					dB	$V_{DS} = 15V$ $V_{G2S} = 10V$ $I_D = 18mA$	
					17	20				
NF	Noise Figure		5.0	6.0				dB		
						1.5	2.5			
$AGC(V_{G2S})$	Range of Automatic Gain Control		40					dB		
						50				
E_{INT}	Interfering Signal at Gate for 1% Cross-Modulation Distortion (Peak Voltage ref. to 50 ohm system)		200					mV	$V_{DS} = 15V$ $V_{G2S} = 10V$ $I_D = 18mA$	
G_{psc}	Conversion Power Gain ($I_D = 8mA$)				14	17		dB		

N-CHANNEL ENHANCEMENT-MODE DUAL D-MOS FET

ORDERING INFORMATION

TO-78 Hermetic Package	SD411HD
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FEATURES

- Normally OFF Configuration
- Low Interelectrode Capacitances
- High-Speed Switching
- Pin Compatible to Industry Standard Dual J-FETs with addition of Substrate Bias Pin

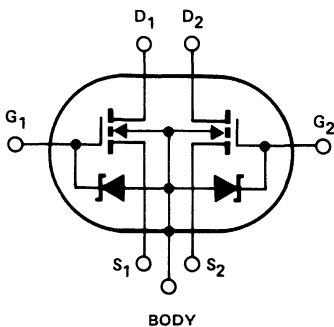
APPLICATIONS

- High-Speed Analog Comparators
- Wide-Band Differential Amplifiers
- Cascode Amplifiers
- High Intercept Point Balanced Mixers

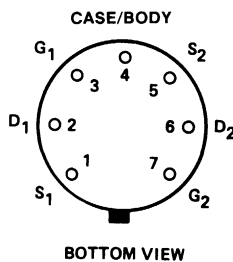
ABSOLUTE MAXIMUM RATINGS (per side, $T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DS} Drain-Source Voltage	+20V	I_D Continuous Drain Current	+50 mA
V_{SD} Source-Drain Voltage	+10V	P_D Device Dissipation (each side)	360 mW
V_{DB} Drain-Body Voltage	+25V	Derating Factor	2.88 mW/ $^\circ\text{C}$
V_{SB} Source-Body Voltage	+15V	P_D Total Device Dissipation	500 mW
V_{GD} Gate-Drain Voltage	+25V	Derating Factor	4 mW/ $^\circ\text{C}$
V_{GS} Gate-Source Voltage	+25V	T_j Operating Junction	
V_{GB} Gate-Body Voltage	+25V	Temperature Range	-55 to +150 $^\circ\text{C}$
V_{G1G2} Gate-to-Gate Voltage	+25V	T_s Storage Temperature Range	-55 to +150 $^\circ\text{C}$
V_{D1D2} Drain-to-Drain Voltage	+20V	T_L Lead Temperature (1/16" from mounting surface for 10 sec.)	+260 $^\circ\text{C}$
V_{S1S2} Source-to-Source Voltage	+15V		

SCHEMATIC DIAGRAM



PIN CONFIGURATION



PACKAGE DIMENSIONS TO-78

(See Package 4)

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$, per side, unless otherwise noted)

#		CHARACTERISTIC	MIN	TYP	MAX	UNITS	TEST CONDITIONS
1	S T A T I C	BV_{DS} Drain Source Breakdown Voltage	20			V	$I_D = 10\text{ nA}$, $V_{GS} = V_{BS} = -5\text{V}$
2		BV_{SD} Source-Drain Breakdown Voltage	10				$I_S = 10\text{ nA}$, $V_{GD} = V_{BD} = -5\text{V}$
3		BV_{DB} Drain-Body Breakdown Voltage	25				$I_D = 10\text{ nA}$, $V_{GB} = 0$ Source Open
4		BV_{SB} Source-Body Breakdown Voltage	15				$I_S = 10\mu\text{A}$, $V_{GB} = 0$ Drain open
5		I_{DSX} Drain-Source Leakage Current		0.7	10	nA	$V_{DS} = 20\text{V}$, $V_{GS} = V_{BS} = -5\text{V}$
6		I_{GBS} Gate-Body Leakage Current			1.0	μA	$V_{GS} = 25\text{V}$, $V_{DB} = V_{SB} = 0$
7		$V_{GS(th)}$ Gate-Source Threshold Voltage	0.5	1.0	2.0	V	$I_D = 1.0\mu\text{A}$, $V_{DS} = V_{GS}$, $V_{SB} = 0$
8		$r_{DS(ON)}$ Drain-Source ⁽¹⁾ ON Resistance			70	ohms	$I_D = 1.0\text{mA}$, $V_{GS} = 5.0\text{V}$, $V_{SB} = 0$
9	D Y N A M I C	g_{fs} Common-Source ⁽¹⁾ Forward Transcond.	10	12		mmhos	$V_{DS} = 10\text{V}$, $I_D = 20\text{mA}$, $V_{SB} = 0$ $f = 1\text{KHz}$
10		C_{iss} Common-Source Input Capacitance		3.5		pF	$V_{DS} = 10\text{V}$ $V_{GS} = V_{BS} = 0$ $f = 1\text{MHz}$
11		C_{oss} Common-Source Output Capacitance		1.2			
12		C_{rbs} Common Source Reverse Transfer Capacitance		0.3			
13	$C_{(gs + sb)}$ Source Node Capacitance		4.5				
14	M A T C H	$ V_{GS1} - V_{GS2} $ Differential Gate Source Voltage		25		mV	$V_{DS} = 10\text{V}$ $I_D = 5.0\text{ mA}$ $V_{SB} = 0$
15		$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$ Differential Drift		25			

Note 1: Pulse Test, $80\mu\text{sec}$, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS: See SD5000 Data Sheet

N-CHANNEL ENHANCEMENT-MODE HIGH-VOLTAGE D-MOS POWER FETS

ORDERING INFORMATION

TO-205AF (TO-39)	TO-226AA (TO-92)	TO-206AA (TO-18)
TO-205AF (TO-39)	TO-226AA (TO-92)	TO-206AA (TO-18)
TO-205AF (TO-39)	TO-226AA (TO-92)	TO-206AA (TO-18)
TO-205AF (TO-39)	TO-226AA (TO-92)	TO-206AA (TO-18)
TO-205AF (TO-39)	TO-226AA (TO-92)	TO-206AA (TO-18)
TO-205AF (TO-39)	TO-226AA (TO-92)	TO-206AA (TO-18)
TO-205AF (TO-39)	TO-226AA (TO-92)	TO-206AA (TO-18)
TO-205AF (TO-39)	TO-226AA (TO-92)	TO-206AA (TO-18)
TO-205AF (TO-39)	TO-226AA (TO-92)	TO-206AA (TO-18)
TO-205AF (TO-39)	TO-226AA (TO-92)	TO-206AA (TO-18)

FEATURES

- Gate Stand-off, $\pm 40V$ min.
- P-channel complements available, VP0540 series
- Wide variety of Packages

APPLICATIONS

- Motor Controls
- Line Drivers
- Power Supplies

ABSOLUTE MAXIMUM RATINGS ($T_C = +25^\circ C$ unless otherwise noted)

Drain-Source Voltage			
SD1100	450V	
SD1101	400V	
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)			
SD1100	450V	
SD1101	400V	
Gate-Source Voltage			
.....	$\pm 40V$	
Continuous Drain Current			
	$T_C = +100^\circ C$	$T_C = +25^\circ C$	
SD1100DD	.10A	.17A	
SD1100HD	.21A	.33A	
SD1101BD	.11A	.18A	
SD1101DD	.13A	.21A	
SD1101HD	.26A	.41A	
Peak Pulsed Drain Current			
.....	0.25A	

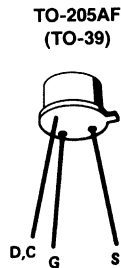
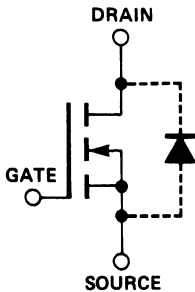
Maximum Power Dissipation

	$T_C = +100^\circ C$	$T_C = +25^\circ C$
HD, TO-39 Pkg.	2.75W	6.88W
BD, TO-92 Pkg.	0.5W	1.35W
DD, TO-18 Pkg.	0.7W	1.80W
Linear Derating Factor		
	Junction to Ambient	Junction to Ambient
	($mW/^\circ C$)	($mW/^\circ C$)
HD, TO-39 Pkg.	36.6	55
BD, TO-92 Pkg.	6.66	10.8
DD, TO-18 Pkg.	9.33	14.4

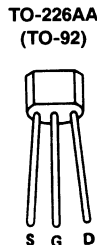
Operating Junction and

Storage Temperature Range	$-55^\circ C$ to $+150^\circ C$
Lead Temperature ($1/16"$ from mounting surface for 10 Sec)	$+260^\circ C$

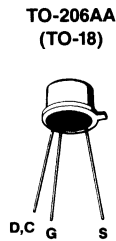
PIN CONFIGURATIONS



See Package 6

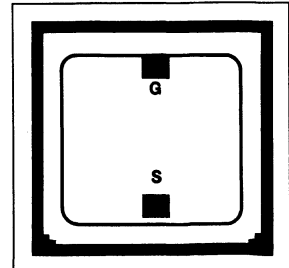


See Package 5



See Package 1

CHIP CONFIGURATION



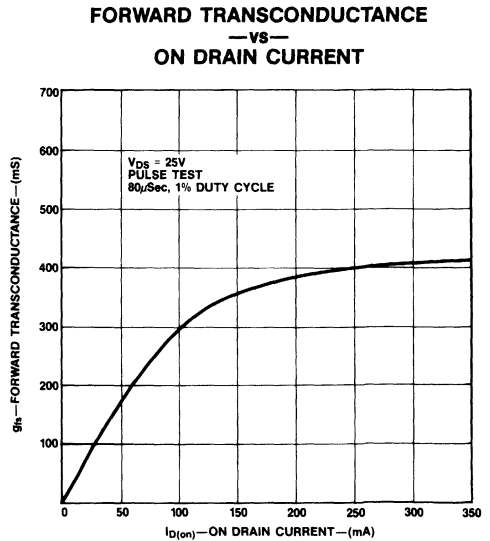
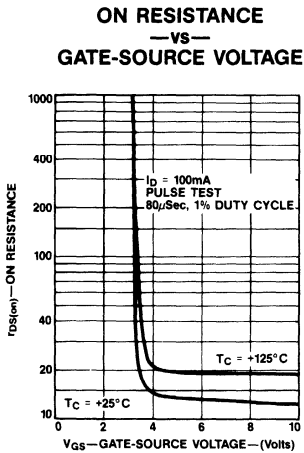
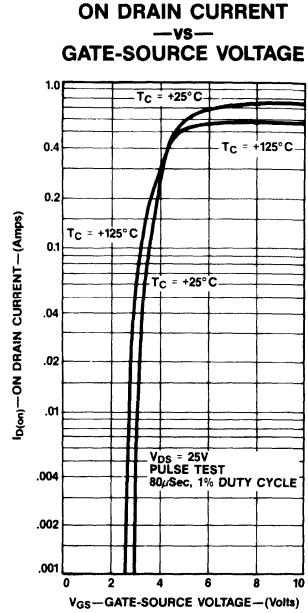
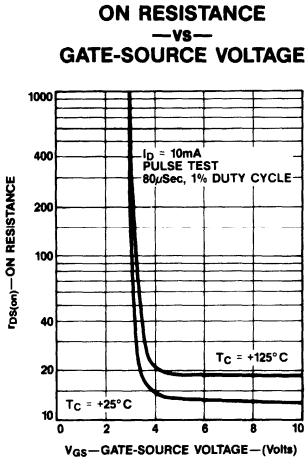
Dimensions: .054 x .051 x .020 in.
Drain is backside contact.

ELECTRICAL CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC		SD1100			SD1101			UNIT	TEST CONDITIONS		
			MIN	TYP	MAX	MIN	TYP	MAX				
1	BV_{DSS}	Drain Source Breakdown Voltage	450	475		400	425		V	$I_D = 10\mu\text{A}, V_{GS} = 0$		
2	I_{GSSF}	Gate Forward Leakage Current		.03	10		.03	10	nA	$V_{GS} = 20\text{V}$	$V_{DS} = 0$	
3	I_{GSSR}	Gate Reverse Leakage Current		-.03	-10		-.03	-10	nA	$V_{GS} = -20\text{V}$		
4	I_{DSS}	Drain-Source OFF Leakage Current		2.0	200				nA	$V_{DS} = 360\text{V}$	$T_C = +125^\circ\text{C}$	
5					2.0				μA	$V_{GS} = 0$		
6								2.0	200	nA	$V_{DS} = 320\text{V}$	$T_C = +125^\circ\text{C}$
7								2.0	μA	$V_{GS} = 0$		
8	$V_{GS(th)}$	Gate Source Threshold Voltage	1.0	3.0	5.0	1.0	3.0	5.0	V	$I_D = 10\mu\text{A}, V_{DS} = V_{GS}$		
9	$I_{D(ON)}$	ON Drain Current ⁽¹⁾	250	750		250	750		mA	$V_{DS} = 25\text{V}, V_{GS} = 10\text{V}$		
10	$r_{DS(ON)}$	Drain-Source ON Resistance ⁽¹⁾		13	35		13	25	ohms	$V_{GS} = 10\text{V}$	$T_C = 125^\circ\text{C}$	
11				19	60		19	42		$I_D = 10\text{mA}$		
12	g_{fs}	Forward Transconductance ⁽¹⁾	250	400		250	400			$V_{DS} = 25\text{V}, I_D = 250\text{mA}$ $f = 1\text{KHz}$		
17	DYNAMIC	C_{iss}		80	100		80	100	pF	$V_{DS} = 25\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$		
18		C_{rss}		1.3	2.5		1.3	2.5				
19		C_{oss}		10.5	15		10.5	15				

Note 1: Pulse Test 80 μSec , 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)



N-CHANNEL ENHANCEMENT-MODE HIGH-VOLTAGE D-MOS POWER FETs

ORDERING INFORMATION



FEATURES

- Gate Stand-off, $\pm 40V$ min.
- Wide variety of Packages
- Low Drain-Source Off Leakage, $I_{DSS} < 200nA$

APPLICATIONS

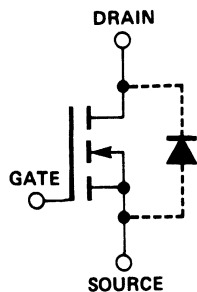
- Motor Controls
- Line Drivers
- Power Supplies

ABSOLUTE MAXIMUM RATINGS ($T_C = +25^\circ C$ unless otherwise noted)

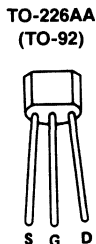
Drain-Source Voltage		
SD1102	250V
SD1112, SD1113	200V
Drain-Gate Voltage		
SD1102	250V
SD1112, SD1113	200V
Gate-Source Voltage		
.....	$\pm 40V$
Continuous Drain Current		
	$T_C = +100^\circ C$	$T_C = +25^\circ C$
SD1102BD, SD1113BD	.17A	.28A
SD1112BD	.20A	.33A
SD1102DD, SD1113DD	.20A	.32A
SD1112DD	.24A	.38A
SD1102HD, SD1113HD	.40A	.63A
SD1112HD	.48A	.76A
Peak Pulsed Drain Current	0.8A

Continuous Device Dissipation		
	$T_C = +100^\circ C$	$T_C = +25^\circ C$
SD1102/1112/1113BD	0.5W	1.35W
SD1102/1112/1113DD	0.7W	1.80W
SD1102/1112/1113HD	2.75W	6.88W
Linear Derating Factor		
	Junction to Ambient	Junction to Ambient
SD1102/1112/1113BD	6.66mW/ $^\circ C$	10.8mW/ $^\circ C$
SD1102/1112/1113DD	9.33mW/ $^\circ C$	14.4mW/ $^\circ C$
SD1102/1112/1113HD	36.6mW/ $^\circ C$	55mW/ $^\circ C$
Operating Junction and Storage Temperature Range		
.....	$-55^\circ C$ to $+150^\circ C$	
Lead Temperature (1/6" from mounting surface for 10 Sec)		
.....	$+260^\circ C$	

PIN CONFIGURATIONS



See Package 6

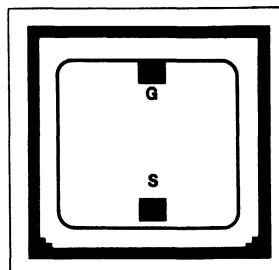


See Package 5



See Package 1

CHIP CONFIGURATION



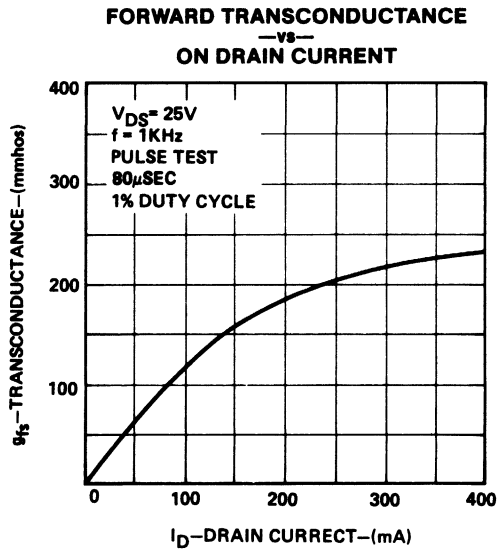
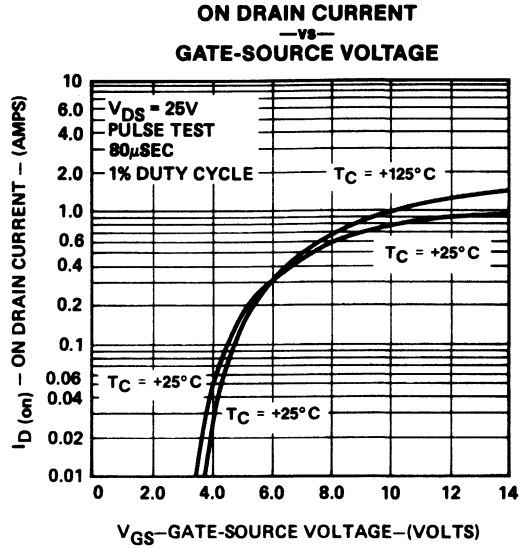
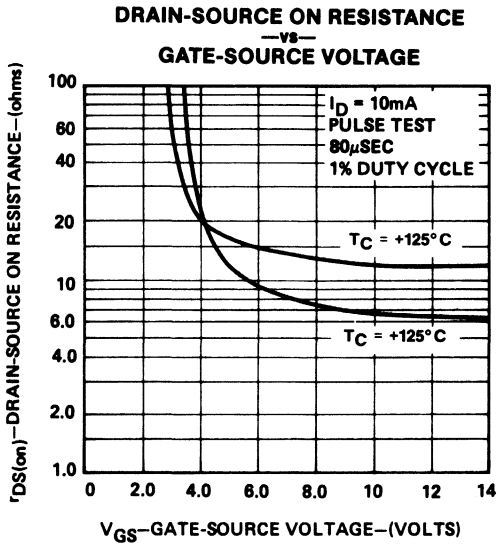
Dimensions: .054 x .051 x .020 in.
Drain is backside contact.

ELECTRICAL CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC		SD1102			SD1112, SD1113			UNIT	TEST CONDITION			
			MIN	TYP	MAX	MIN	TYP	MAX					
1	STATIC	BV_{DSS} Drain Source Breakdown Voltage	250	270		200	250		V	$I_D = 10\mu\text{A}, V_{GS} = 0$			
2		$V_{GS(th)}$ Gate Source Threshold Voltage	1.0	3.0	5.0	1.0	3.0	5.0	V	$V_{DS} = V_{GS}, I_D = 10\mu\text{A}$			
3		I_{GSSF} Gate Forward Leakage Current		.03	10		.03	10	nA	$V_{GS} = 20\text{V}$	$V_{DS} = 0$		
4		I_{GSSR} Gate Reverse Leakage Current		-.03	-10		-.03	-10		$V_{GS} = -20\text{V}$			
5		I_{DSS} Drain-Source OFF Leakage Current		2.0	200				nA	$V_{DS} = 200\text{V}$	$T_C = +125^\circ\text{C}$		
6					2.0				μA	$V_{GS} = 0$			
7							2.0	200	nA	$V_{DS} = 160\text{V}$			
8								2.0	μA	$V_{GS} = 0$			
9		$I_{D(ON)}$ ON Drain Current ¹	0.8	1.0		0.5	1.0		A	$V_{DS} = 25\text{V}, V_{GS} = 10\text{V}$			
10		$r_{DS(ON)}$ Drain-Source ON Resistance ⁽¹⁾	SD1102	6.6	10				ohms	$V_{GS} = 10\text{V}$ $I_D = 100\text{mA}$	$T_C = 125^\circ\text{C}$		
11				12	17								
12				SD1112				6.6				7.0	$T_C = +125^\circ\text{C}$
13								10				11.9	
14					SD1113							6.6	
15						12	17	$T_C = +125^\circ\text{C}$					
16	DYNAMIC	g_{fs} Common-Source Forward Transcond. ⁽¹⁾	200	300		200	300		mmhos	$V_{DS} = 25\text{V}, I_D = 0.5\text{A}$ $f = 1\text{KHz}$			
17		C_{iss} Common-Source Input Capacitance		80	100		80	100	pF	$V_{DS} = 25\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$			
18		C_{rss} Common-Source Reverse Transfer Capacitance		1.3	2.5		1.3	2.5					
19		C_{oss} Common-Source Output Capacitance		10.5	15		10.5	15					
20		t_{on} Turn ON Time			10			10					
21		t_{off} Turn OFF Time			18			18	ns	$V_{DD} = 60\text{V}, V_{G(on)} = 10\text{V}$ $R_G = 51\Omega, R_L = 68\Omega$			

Note 1: Pulse Test 80 μSec , 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise specified)



N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION



FEATURES

- Inherent Current Sharing Capability when Paralleled
- Simple Straight-Forward DC Biasing
- Extended Safe Operating Area
- Inherently Temperature Stable —
Output Current Decreases as Temperature Increases

APPLICATIONS

- High-Speed Pulse Amplifiers
- Logic Buffers
- Line Drivers
- Solid-State Relays

ABSOLUTE MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Drain-Source Voltage	60V
Drain-Gate Voltage (R _{GS} = 1MΩ)	60V
Gate-Source Voltage	±40V
Continuous Drain Current	
T _C = +100°C	T _C = +25°C
.21A	.34A
Peak Pulsed Current	2.0A
Continuous Device Dissipation	
T _C = +100°C	T _C = +25°C
0.4W	1.0W

Linear Derating Factor

T _C = +100°C	T _C = +25°C
5.3mW/°C	8.0mW/°C

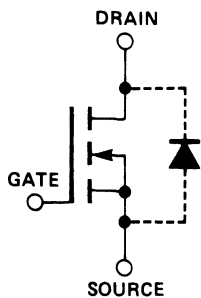
Operating Junction and

Storage Temperature Range

Lead Temperature (1/16" from mounting

surface for 10 Sec)

PIN CONFIGURATIONS



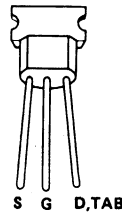
Drain common to Case or Tab.

TO-206AA
(TO-18)



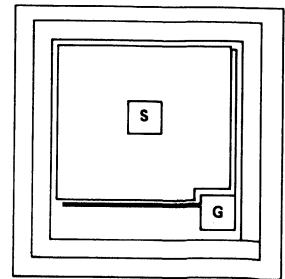
See Package 1

TO-237



See Package 7

CHIP CONFIGURATION



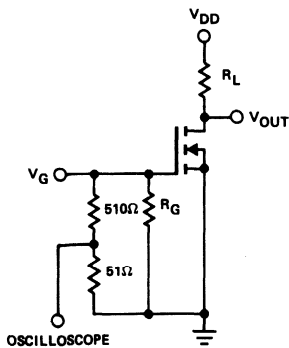
Dimensions: .031 × .032 × .020 Inches
Drain is backside contact.

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC	SD1106			UNIT	TEST CONDITION
		MIN	TYP	MAX		
1	BV _{DSS} Drain-Source Breakdown Voltage	60			V	$I_D = 100\mu\text{A}$, $V_{GS} = 0$
2	V _{GS(th)} Gate-Source Threshold Voltage	0.8		2.5	V	$V_{DS} = V_{GS}$, $I_D = 1\text{mA}$
3	I _{GBS} Gate-Body Leakage Current		.03	10	nA	$V_{GS} = 20\text{V}$, $V_{DS} = 0$
4	I _{DSS} Drain-Source OFF Leakage Current		.01	10	μA	$V_{DS} = 40\text{V}$, $V_{GS} = 0$
5	I _{D(on)} ON Drain Current	0.25			A	$V_{DS} = 25\text{V}$ (Note 1)
6		0.50				
7	V _{DS(on)} Drain-Source ON Voltage		1.8	2.5	v	$V_{GS} = 10\text{V}$, $I_D = 0.5\text{A}$ (Note 1)
8	g _{fs} Common-Source Forward Transcond.	100	270		mmhos	$V_{DS} = 15\text{V}$, $I_D = 0.5\text{A}$ $f = 1\text{KHz}$ (Note 1)
9	C _{iss} Common-Source Input Capacitance		80		pF	$V_{DS} = 25\text{V}$, $V_{GS} = 0$ $f = 1\text{MHz}$
10	C _{rss} Common-Source Reverse Transfer Capacitance		1.3			
11	C _{oss} Common-Source Output Capacitance		10.5			
12	t _{on} Turn-On Time		4.0	6.0	nSec	$V_{DD} = 25\text{V}$ $R_L = 25\text{ ohms}$ $R_G = 51\text{ ohms}$ $V_{G(on)} = 10\text{V}$
13	t _{off} Turn-Off Time		4.0	6.0		

Note 1: Pulse Test 80 μSec , 1% Duty Cycle

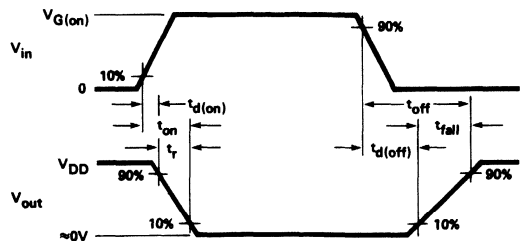
SWITCHING TIMES TEST CIRCUIT



INPUT PULSE
 $t_r < 0.5\text{ nSEC}$
PULSE WIDTH - 100 nSEC

SAMPLING OSCILLOSCOPE
 $t_r < 0.36\text{ nSEC}$
 $R_{in} > 1\text{M}\Omega$
 $C_{in} < 2.0\text{ pF}$

TEST WAVEFORMS



N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION

Part No.	Package	Drain	Gate	Part No.	Package	Drain	Gate
SD1107	TO-18	—	—	SD1107N	TO-18	—	—
SD1117	TO-18	—	—	SD1117N	TO-18	—	—
SD1107	TO-226AA	—	—	SD1107N	TO-226AA	—	—
SD1117	TO-226AA	—	—	SD1117N	TO-226AA	—	—
SD1107	14-Pin Plastic DIP	—	—	SD1107N	14-Pin Plastic DIP	—	—
		100V, 4.0 ohm				60V, 2.5 ohm	

FEATURES

- Gate Standoff Voltage, $\pm 40V$ min.
- Available in a wide variety of packages
- Low Capacitance
- Low ON Resistance
- P-Channel Complements Available, SD2107

APPLICATIONS

- High-Speed Pulse Amplifiers
- CMOS Logic to High-Current Interfaces
- High-Speed Switching
- Line Drivers

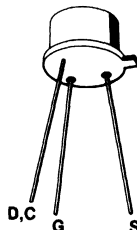
PIN CONFIGURATIONS

TO-206AA
(TO-18)



(See Package 1)

TO-205AF
(TO-39)



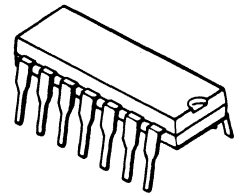
(See Package 6)

TO-226AA
(TO-92)

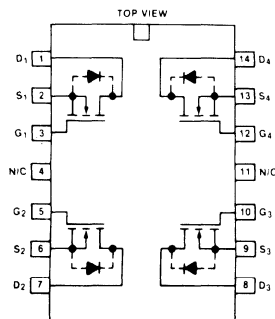
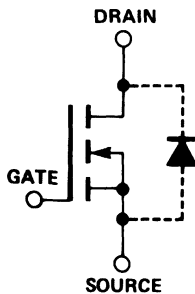


(See Package 5)

14-Pin Plastic DIP

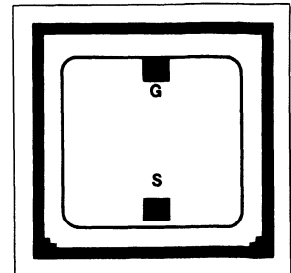


(See Package 9)



SD1107N SD1117N
4 Isolated Chips per Package

CHIP CONFIGURATION



Dimensions: .054 x .051 x .020 in.
Drain is backside contact.

ABSOLUTE MAXIMUM RATINGS Single Units ($T_C = +25^\circ\text{C}$ unless otherwise noted)

Drain-Source Voltage			Maximum Power Dissipation		
SD1107	100V			$T_C = +100^\circ\text{C}$	$T_C = +25^\circ\text{C}$
SD1117	60V		HD, TO-39 Pkg.	2.75W	6.88W
Drain-Gate Voltage ($R_{GS} = 1\text{M}\Omega$)			BD, TO-92 Pkg.	0.5W	1.35W
SD1107	100V		DD, TO-18 Pkg.	0.7W	1.80W
SD1117	60V		Linear Derating Factor		
Gate-Source Voltage	$\pm 40\text{V}$			Junction to Ambient	Junction to Ambient
Continuous Drain Current				($\text{mW}/^\circ\text{C}$)	($\text{mW}/^\circ\text{C}$)
	$T_C = +100^\circ\text{C}$	$T_C = +25^\circ\text{C}$			
SD1107BD	0.3A	0.4A	HD, TO-39 Pkg.	36.6	55
SD1107DD	0.4A	0.5A	BD, TO-92 Pkg.	6.66	10.8
SD1107HD	0.6A	1.0A	DD, TO-18 Pkg.	9.33	14.4
SD1117BD	0.3A	0.5A	Operating Junction and		
SD1117DD	0.4A	0.6A	Storage Temperature Range	-55°C to +150°C	
SD1117HD	0.8A	1.2A	Lead Temperature (1/16" from mounting		
Peak Pulsed Drain Current	2.0A		surface for 10 Sec)	+260°C	

ABSOLUTE MAXIMUM RATINGS Quad Units in 14-Pin Plastic DIP Package ($T_C = +25^\circ\text{C}$ unless otherwise noted)

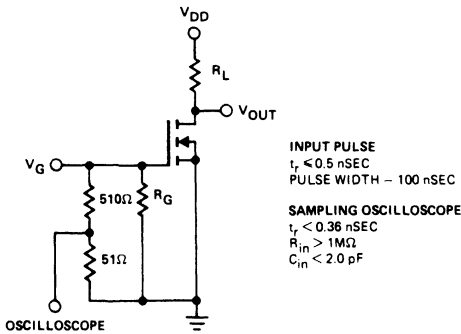
Drain-Source Voltage			Peak Pulsed Drain Current	2.0A	
SD1107N	100V		Continuous Device Dissipation		
SD1117N	60V			$T_C = +85^\circ\text{C}$	$T_C = +25^\circ\text{C}$
Drain-Gate Voltage ($V_{GS} = 0$)			Total Package	.64W	2.0W
SD1107N	100V		Single Device	.30W	1.0W
SD1117N	60V			$T_A = +25^\circ\text{C}$	$T_C = +25^\circ\text{C}$
Gate-Source Voltage	$\pm 0\text{V}$		Total Package	10.6mW/°C	20mW/°C
Continuous Drain Current			Single Device	5.0mW/°C	10mW/°C
	$T_C = +85^\circ\text{C}$	$T_C = +25^\circ\text{C}$	Operating Junction		
Total Package			Temperature Range	-55°C to +125°C	
SD1107N	0.3A	0.5A	Storage Temperature Range	-55°C to +125°C	
SD1117N	0.4A	0.7A	Lead Temperature (1/16" from mounting		
Single Device			surface for 10 Sec)	+260°C	
SD1107N	0.2A	0.3A			
SD1117N	0.3A	0.5A			

ELECTRICAL CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise noted)

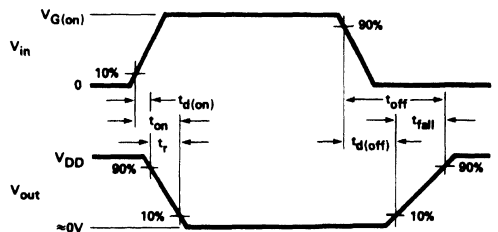
#	CHARACTERISTIC		SD1107			SD1117			UNIT	TEST CONDITIONS		
			MIN	TYP	MAX	MIN	TYP	MAX				
1	BV_{DSS}	Drain Source Breakdown Voltage	100	130		60	90		V	$I_D = 10\mu\text{A}, V_{GS} = 0$		
2	I_{GSSF}	Gate Forward Leakage Current		.03	10		.03	10	nA	$V_{GS} = 20\text{V}$	$V_{DS} = 0$	
3	I_{GSSR}	Gate Reverse Leakage Current		-.03	-10		-.03	-10		$V_{GS} = -20\text{V}$		
4	I_{DSS}	Drain-Source OFF Leakage Current		2.0	200				nA	$V_{DS} = 80\text{V}$ $V_{GS} = 0$	$T_C = +125^\circ\text{C}$	
5					2.0				μA			
6								2.0	200	nA	$V_{DS} = 48\text{V}$ $V_{GS} = 0$	$T_C = +125^\circ\text{C}$
7								2.0	μA			
8	$V_{GS(th)}$	Gate Source Threshold Voltage	0.8		2.0	0.8		2.0	V	$I_D = 1\text{mA}, V_{DS} = V_{GS}$		
9	$I_{D(ON)}$	ON Drain Current ⁽¹⁾	2.0	3.0		2.0	3.0		A	$V_{DS} = 10\text{V}, V_{GS} = 10\text{V}$		
10	$r_{DS(ON)}$	Drain-Source ON Resistance ⁽¹⁾		3.0	5.0		3.0	4.5	ohms	$V_{GS} = 5\text{V}$ $I_D = 0.3\text{A}$	$T_C = 125^\circ\text{C}$	
11					8.5			7.6				
12					1.9	4.0		1.9		2.5	$V_{GS} = 10\text{V}$ $I_D = 1.0\text{A}$	$T_C = +125^\circ\text{C}$
13						6.8				4.3		
14	g_{fs}	Forward Transconductance ⁽¹⁾	400	580		400	580		mS	$V_{DS} = 10\text{V}, I_D = 0.5\text{A}$ $f = 1\text{KHz}$		
15	C_{iss}	Common-Source Input Capacitance		80	100		80	100	pF	$V_{DS} = 25\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$		
16	C_{rss}	Common-Source Reverse Transfer Capacitance		1.3	2.5		1.3	2.5				
17	C_{oss}	Common-Source Output Capacitance		10.5	15		10.5	15				
18	t_{on}	Turn-On Time		4.0	6.0		4.0	6.0	nSec	$V_{DD} = 25\text{V}, R_L = 25\text{ ohms}$ $R_G = 51\text{ ohms}, V_{G(on)} = 10\text{V}$		
19	t_{off}	Turn-Off Time		4.0	6.0		4.0	6.0				

Note 1: Pulse Test 80 μSec , 1% Duty Cycle

SWITCHING TIMES TEST CIRCUIT

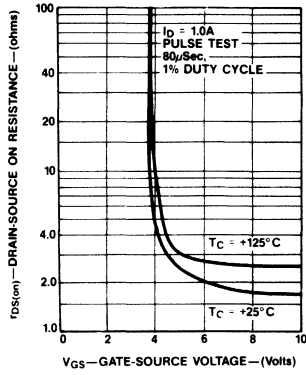


TEST WAVEFORMS

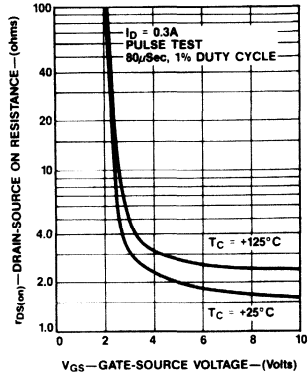


TYPICAL PERFORMANCE CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise noted)

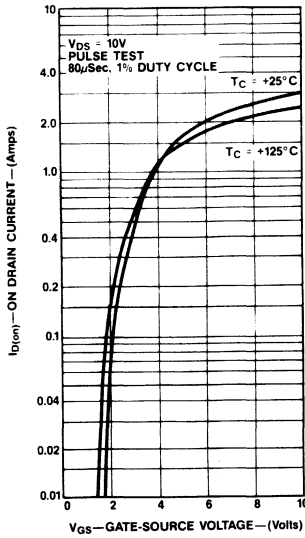
DRAIN-SOURCE ON RESISTANCE
—vs—
GATE-SOURCE VOLTAGE



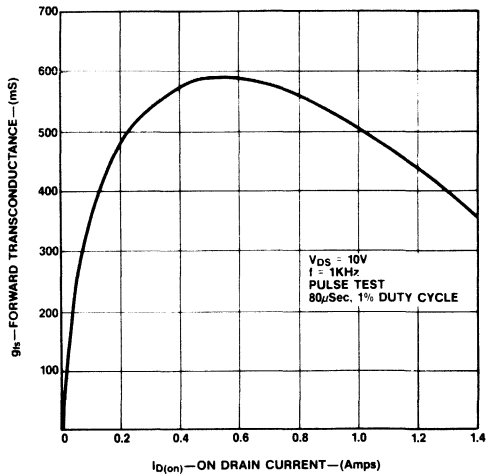
DRAIN-SOURCE ON RESISTANCE
—vs—
GATE-SOURCE VOLTAGE



ON DRAIN CURRENT
—vs—
GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE
—vs—
ON DRAIN CURRENT



N-CHANNEL ENHANCEMENT-MODE HIGH-VOLTAGE D-MOS POWER FETS

ORDERING INFORMATION

Lead Form in TO-92 Case	SD1122CHP
Lead Form in TO-92 Pin Lead Formed	SD1122BD
Description	200V, 10 ohms

FEATURES

- Inherent Current Sharing Capability when Paralleled
- Simple Straight-Forward DC Biasing
- Extended Safe Operating Area
- Inherently Temperature Stable — Output Current Decreases as Temperature Increases

APPLICATIONS

- High-Speed Pulse Amplifiers
- Logic Buffers
- Line Drivers
- Line Interrupters
- Output Switches
- Display Drivers

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

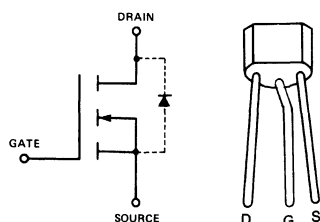
Drain-Source Voltage	200V
Drain-Gate Voltage ($V_{GS} = 0$)	200V
Gate-Source Voltage	$\pm 30\text{V}$
Continuous Device Dissipation (Note 2)	0.3W
Linear Derating Factor (Note 2)	2.4mW/ $^\circ\text{C}$
Continuous Drain Current (Note 2)	0.12A
Peak Drain Current (Note 1, Note 2)	0.5A
Continuous Device Dissipation (Note 1, Note 2)	1.0W
Linear Derating Factor (Note 1, Note 2)	8.0mW/ $^\circ\text{C}$

Thermal Resistance, Junction to case	125 $^\circ\text{C}/\text{W}$
Operating Junction Temperature Range	-55 to +150 $^\circ\text{C}$
Storage Temperature Range	-55 to +150 $^\circ\text{C}$
Lead Temperature (1/16" from mounting surface for 30 Sec)	+260 $^\circ\text{C}$

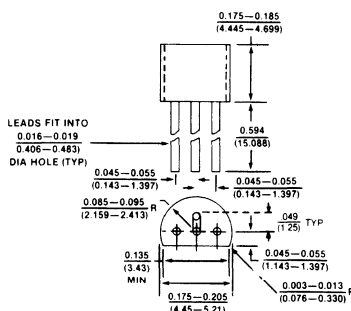
Note 1: $T_{CASE} = +25^\circ\text{C}$

Note 2: Not applicable to chips. Final value depends upon mounting substrate.

SCHEMATIC DIAGRAM

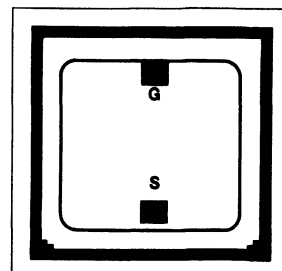


PACKAGE DIMENSIONS TO-92, LEAD FORMED



Lead-formed to TO-18 pin circle.
All dimensions in inches and (millimeters)

CHIP CONFIGURATION



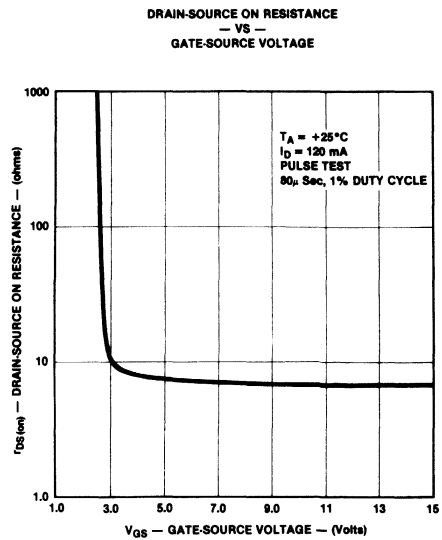
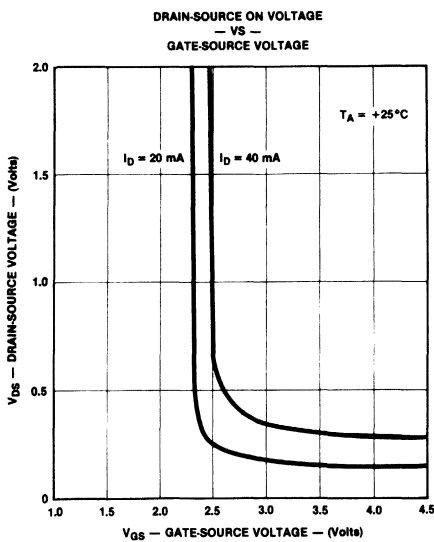
Dimensions: .054 x .051 x .020 in.
Drain is backside contact.

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC		SD1122			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
1	STATIC	$B_{V_{DS}}$ Drain Source Breakdown Voltage	200	270		V	$I_D = 10\mu\text{A}, V_{GS} = 0$	
2		$V_{GS(th)}$ Gate Source Threshold Voltage	0.8	1.9	2.4	V	$V_{DS} = V_{GS}, I_D = 1\text{mA}$	
3		I_{GBS} Gate-Body Leakage Current		.03	1.0	nA	$V_{GS} = 20\text{V}, V_{DS} = 0$	
4		I_{DSX} Drain-Source OFF Leakage Current	I_{DSS} Drain-Source OFF Leakage Current		0.1	1.0	μA	$V_{DS} = 70\text{V}, V_{GS} = 0.2\text{V}$
5						30	nA	$V_{DS} = 130\text{V}, V_{GS} = 0$
6		$I_{D(on)}$ ON Drain Current	0.5			A	$V_{DS} = 25\text{V}, V_{GS} = 15\text{V}$ (Note 1)	
7		$r_{DS(on)}$ Static Drain-Source ON Resistance		7.5	10	ohms	$I_D = 120\text{mA}$ (Note 1), $V_{GS} = 5.0\text{V}$	
8				11	28			
9		DYNAMIC	g_{fs} Common-Source Forward Transcond.		300		mmhos	$V_{DS} = 25\text{V}, I_D = 0.5\text{A}$ $f = 1\text{KHz}$ (Note 1)
10			C_{iss} Common-Source Input Capacitance		80		pF	$V_{DS} = 25\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$
11			C_{rss} Common-Source Reverse Transfer Capacitance		1.3			
12			C_{oss} Common-Source Output Capacitance		10.5			

Note 1: Pulse Test $80\mu\text{Sec}$, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS



N-CHANNEL ENHANCEMENT-MODE VERTICAL D-MOS FET ULTRA LOW-LEAKAGE

ORDERING INFORMATION

TO-226AA (TO-92) Plastic Package	SD1127BD
Chip in Tube Pack	SD1127CHP
Description	60 Volt, 4.0 ohm

FEATURES

- Drain-Source Leakage (I_{DSS}), 1.0nA max
- Low Output and Transfer Capacitances
- Extended Safe Operating Area

APPLICATIONS

- High-Speed Switches
- Low-Leakage Solid State Relays
- High-Speed Pulse Amplifiers
- Logic Interfaces
- Line Drivers

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Drain-Source Voltage	+60V	
Drain-Gate Voltage ($V_{GS} = 0$)	+60V	
Gate-Source Voltage	$\pm 30\text{V}$	
Continuous Drain Current	$T_A = +25^\circ\text{C}$	$T_C = +25^\circ\text{C}$
SD1127BD	.20A	.36A
Peak Pulsed Drain Current	2.0A	

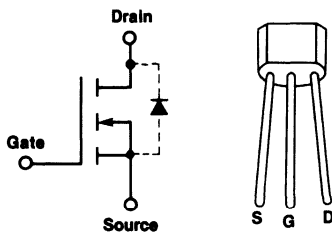
Continuous Device Dissipation

	$T_A = +25^\circ\text{C}$	$T_C = +25^\circ\text{C}$
SD1127BD	0.30W	1.0W
Linear Derating Factor	$T_A = +25^\circ\text{C}$	$T_C = +25^\circ\text{C}$
SD1127BD	3.0mW/ $^\circ\text{C}$	10mW/ $^\circ\text{C}$

Operating Junction and Storage Temperature Range
-55°C to +150°C

Lead Temperature (1/16" from mounting surface
for 30 sec.) +260°C

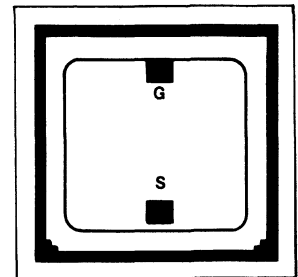
PIN CONFIGURATION



PACKAGE DIMENSIONS (TO-92) TO-226AA

(See Package 5)

CHIP CONFIGURATION



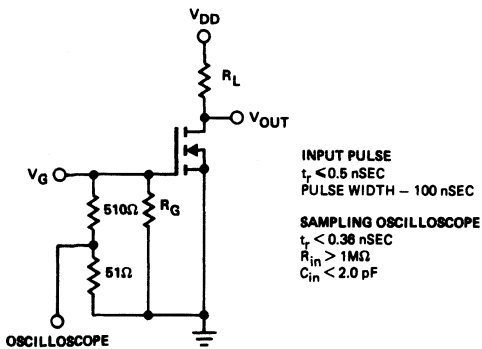
Dimensions: .054 x .051 x .020 in.
Drain is backside contact.

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

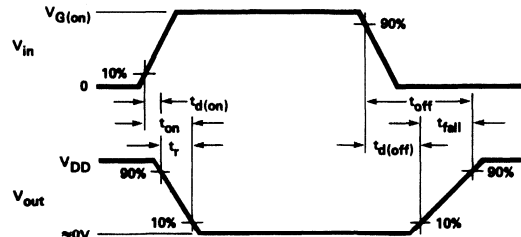
#	CHARACTERISTIC	SD1127			UNIT	TEST CONDITION
		MIN	TYP	MAX		
1	BV_{DSS} Drain-Source Breakdown Voltage	60	90		V	$I_D = 10\mu\text{A}$, $V_{GS} = 0$
2	$V_{GS(th)}$ Gate-Source Threshold Voltage	0.8		2.4	V	$V_{DS} = V_{GS}$, $I_D = 1\text{mA}$
3	I_{GBS} Gate-Body Leakage Current		.03	1.0	nA	$V_{GS} = 20\text{V}$, $V_{DS} = 0$ $T_A = +125^\circ\text{C}$
4				10		
5	I_{DSS} Drain-Source OFF Leakage Current			1.0	nA	$V_{DS} = 30\text{V}$, $V_{GS} = 0$ $T_A = +125^\circ\text{C}$
6				100		
7	$I_{D(on)}$ ON Drain Current	2.0	3.5		A	$V_{DS} = 25\text{V}$, $V_{GS} = 10\text{V}$ (Note 1)
8	$r_{DS(on)}$ Drain-Source ON Resistance		3.2	5.0	ohms	$V_{GS} = 5\text{V}$, $I_D = 0.3\text{A}$ (Note 1) $V_{GS} = 10\text{V}$, $I_D = 1.0\text{A}$ (Note 1)
9			2.9	4.0		
10	g_{fs} Common-Source Forward Transcond.	250	500		mmhos	$V_{DS} = 25\text{V}$, $I_D = 1.0\text{A}$ $f = 1\text{KHz}$ (Note 1)
11	C_{iss} Common-Source Input Capacitance		80		pF	$V_{DS} = 25\text{V}$, $V_{GS} = 0$ $f = 1\text{MHz}$
12	C_{rss} Common-Source Reverse Transfer Capacitance		1.5			
13	C_{oss} Common-Source Output Capacitance		15			
14	t_{on} Turn-On Time		4.0	6.0	nSec	$V_{DD} = 25\text{V}$ $R_L = 25\text{ ohms}$ $R_G = 51\text{ ohms}$ $V_{G(on)} = 10\text{V}$
15	t_{off} Turn-Off Time		4.0	6.0		

Note 1: Pulse Test 80µSec, 1% Duty Cycle

SWITCHING TIMES TEST CIRCUIT



TEST WAVEFORMS



N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION



FEATURES

- Low Threshold, $V_{GS(th)}$ 1.5V max
- Low Output and Transfer Capacitance
- Extended Safe Operating Area
- Complementary P-Channel Drivers Available

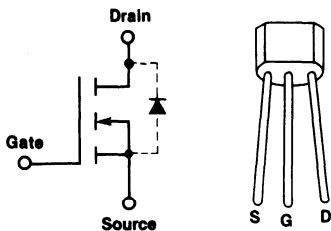
APPLICATIONS

- Complementary Voltage and Current Drivers
- Line Drivers
- Pulse Amplifiers
- Solid-State Relays

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

Drain-Source Voltage			Peak Pulsed Drain Current	+2.0A	
SD1137, TN0106	+60V		Continuous Device Dissipation		
TN0110	+100V		$T_A = +25^\circ\text{C}$	$T_C = +25^\circ\text{C}$	
SD1137, TN0106	+60V		TO-92 (N3 & BD) pkg	0.30W	1.0W
TN0110	+100V		Linear Derating Factor		
Gate-Source Voltage	$\pm 30\text{V}$		$T_A = +25^\circ\text{C}$	$T_C = +25^\circ\text{C}$	
Continuous Drain Current	$T_A = +25^\circ\text{C}$	$T_C = +25^\circ\text{C}$	TO-92 (N3 & BD) pkg	3.0mW/ $^\circ\text{C}$	10mW/ $^\circ\text{C}$
SD1137BD	.25A	.46A	Operating Junction and Storage Temperature Range	-55 $^\circ\text{C}$ to +150 $^\circ\text{C}$	
TN0106N3 } TN0110N3 }	.23A	.42A	Lead Temperature (1/16" from mounting surface for 30 sec)	+250 $^\circ\text{C}$	

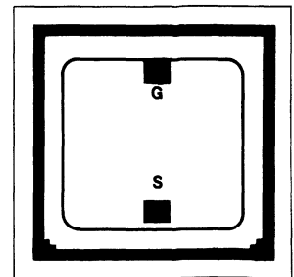
PIN CONFIGURATION



PACKAGE DIMENSIONS (TO-92) TO-226AA

(See Package 5)

CHIP CONFIGURATION



Dimensions: .054 x .051 x .020 in.
Drain is backside contact.

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

#	PARAMETER	SD1137			TNO106			TNO110			UNIT	CONDITIONS		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX				
1	BV_{DSS} Drain-Source Breakdown Voltage	60	90		60	90		100	115		V	$I_D = 1.0\text{mA}, V_{GS} = 0$		
2	I_{DSS} Drain-Source Off Leakage Current			100							μA	$V_{DS} = 48\text{V}$	$T_A = +125^\circ\text{C}$ $V_{GS} = 0$	
3							500					$V_{DS} = 48\text{V}$		
4										500		$V_{DS} = 80\text{V}$		
5			.01	1.0								$V_{DS} = 60\text{V}$	$V_{GS} = 0$	
6						.01	10					$V_{DS} = 60\text{V}$		
7									.01	10		$V_{DS} = 100\text{V}$		
8		I_{GBS} Gate-Body Leakage Current			± 1.0			± 1.0				± 1.0	μA	$V_{GB} = \pm 30\text{V}$
9				1.0			10			10	nA	$V_{GB} = \pm 20\text{V}$		
10	$V_{GS(th)}$ Gate-Source Threshold Voltage	0.5		1.5	0.5		1.5	0.5		1.5	V	$V_{DS} = V_{GS}, I_D = 1.0\text{mA}$		
11	$r_{DS(on)}$ Drain-Source On Resistance			4.5			4.5			4.5	ohms	$V_{GS} = 5\text{V}, I_D = .25\text{A}$	(Note 1)	
12				2.5								$V_{GS} = 10\text{V}$		$I_D = 1.0\text{A}$
13							3.0			3.0				$I_D = 0.5\text{A}$
14	$I_{D(on)}$ On Drain Current			.75			.75			.75	A	$V_{GS} = 5\text{V}$		$V_{DS} = 25\text{V}$
15			2.0		2.0			2.0		2.0		$V_{GS} = 10\text{V}$		
16	g_{fs} Common-Source Forward Transcond.	300	500								mmhos	$V_{DS} = 25\text{V}$		$I_D = 0.5\text{A}$
17					225	500		225	500			$V_{DS} = 20\text{V}$	$f = 1\text{KHz}$	
18	V_{SD} Source-Drain Forward Voltage			1.5							V	$I_{SD} = 0.8\text{A}$	$V_{GS} = 0$	
19							1.5		1.5			$I_{SD} = 0.5\text{A}$		
20	C_{iss} Common-Source Input Capacitance			60			60			60	pF	$V_{DS} = 25\text{V}$ $V_{GS} = 0$ $f = 1\text{MHz}$		
21	C_{oss} Common-Source Output Capacitance		11	35		11	35		11	35				
22	C_{rss} Common-Source Reverse Transfer Capacitance		1.5	8.0		1.5	8.0		1.5	8.0				
23	t_{on} Turn ON Time		8.0	10		8.0	10		8.0	10	nS	$V_{DD} = 25\text{V}, V_{G(on)} = 10\text{V}$ $R_G = 51\Omega, R_L = 25\Omega$		
24	t_{off} Turn OFF Time		8.0	12		8.0	12		8.0	12				

NOTE 1: Pulse Test, 80 μ Sec, 1% Duty Cycle

N-CHANNEL ENHANCEMENT-MODE HIGH-VOLTAGE D-MOS FETs

ORDERING INFORMATION



FEATURES

- Gate Stand-off Voltage, $\pm 40\text{V}$ min.
- P-Channel Complements Available, SD2204
- Low Capacitance (C_{OSS} 1.0pF typ.)
- Low Leakage

APPLICATIONS

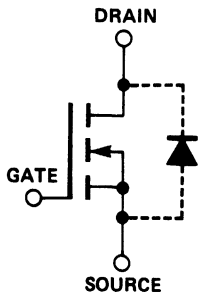
- High-Voltage Level Translators
- High-Voltage Display Drivers
- High-Voltage Switches
- AC-DC Relays

ABSOLUTE MAXIMUM RATINGS ($T_C = +25^\circ\text{C}$ unless otherwise noted)

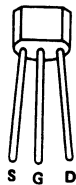
Drain-Source Voltage		
SD1200		450V
SD1201		400V
Drain-Gate Voltage ($R_{GS} = 1\text{M}\Omega$)		
SD1200		450V
SD1201		400V
Gate-Source Voltage		
		$\pm 40\text{V}$
Continuous Drain Current		
	$T_C = +100^\circ\text{C}$	$T_C = +25^\circ\text{C}$
SD1200DD	18mA	28mA
SD1201BD	18mA	30mA
SD1201DD	20mA	30mA
Peak Drain Current		
		20mA

Maximum Power Dissipation		
	$T_C = +100^\circ\text{C}$	$T_C = +25^\circ\text{C}$
BD, TO-92 Pkg.	0.3W	0.8W
DD, TO-18 Pkg.	0.4W	1.0W
Linear Derating Factor		
	Junction to Ambient	Junction to Case
	($\text{mW}/^\circ\text{C}$)	($\text{mW}/^\circ\text{C}$)
BD, TO-92 Pkg.	4.0	6.4
DD, TO-18 Pkg.	5.3	8.0
Operating Junction and Storage Temperature Range		
		-55°C to $+150^\circ\text{C}$
Lead Temperature ($1/16''$ from mounting surface for 0 Sec)		
		$+260^\circ\text{C}$

PIN CONFIGURATIONS



TO-226AA
(TO-92)



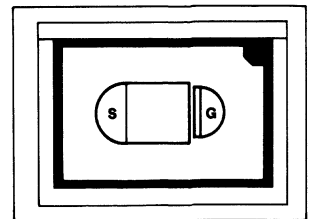
See Package 5

TO-206AA
(TO-18)



See Package 1

CHIP CONFIGURATION



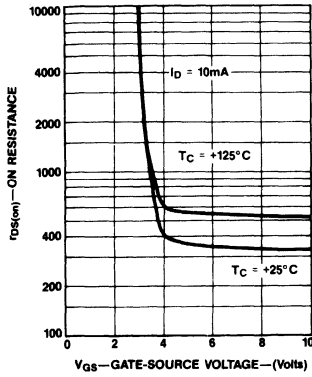
Dimensions: .025 x .035 x .020 in.
Drain is backside contact.

ELECTRICAL CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise noted)

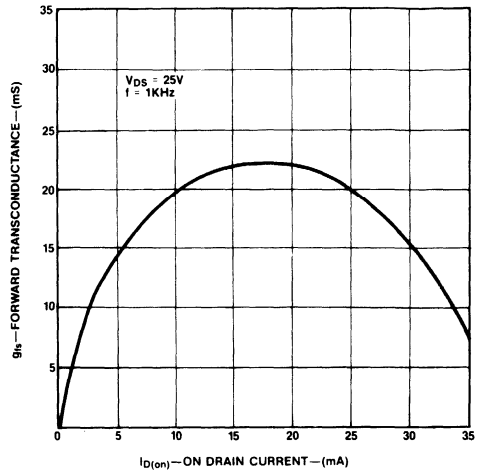
#	CHARACTERISTIC		SD1200			SD1201			UNIT	TEST CONDITIONS	
			MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS} Drain Source Breakdown Voltage	450	475		400	425		V	$I_D = 10\mu\text{A}, V_{GS} = 0$	
2		I_{GSSF} Gate Forward Leakage Current		.03	10		.03	10	nA	$V_{GS} = 20\text{V}$	$V_{DS} = 0$
3		I_{GSSR} Gate Reverse Leakage Current		-.03	-10		-.03	-10		$V_{GS} = -20\text{V}$	
4		I_{DSS} Drain-Source OFF Leakage Current			1.0	100			nA	$V_{DS} = 360\text{V}$	$T_C = +125^\circ\text{C}$
5						1.0			μA	$V_{GS} = 0$	
6							1.0	100	nA	$V_{DS} = 320\text{V}$	
7								1.0	μA	$V_{GS} = 0$	
8		$V_{GS(th)}$ Gate Source Threshold Voltage	1.0	3.0	5.0	1.0	3.0	5.0	V	$I_D = 10\mu\text{A}, V_{DS} = V_{GS}$	
9		$I_{D(ON)}$ ON Drain Current	20	35		20	35		mA	$V_{DS} = 25\text{V}, V_{GS} = 10\text{V}$	
10		$r_{DS(ON)}$ Drain-Source ON Resistance		310	700		310	500	ohms	$V_{GS} = 10\text{V}$	$T_C = 125^\circ\text{C}$
11				520	1200		520	850		$I_D = 10\text{mA}$	
12	DYNAMIC	g_{fs} Forward Transconductance	10	20		10	20		mS	$V_{DS} = 25\text{V}, I_D = 10\text{mA}$ $f = 1\text{KHz}$	
13		C_{iss} Common-Source Input Capacitance		5.0	10		5.0	10	pF	$V_{DS} = 25\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$	
14		C_{rss} Common-Source Reverse Transfer Capacitance		0.8	1.0		0.8	1.0			
11		C_{oss} Common-Source Output Capacitance		1.0	2.0		1.0	2.0			

TYPICAL PERFORMANCE CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise specified)

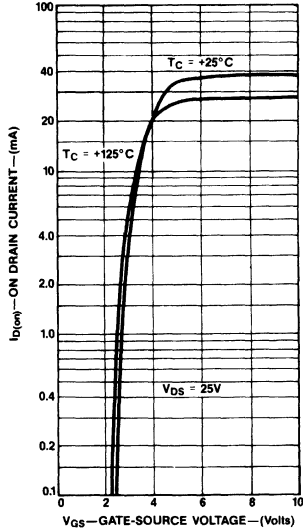
ON RESISTANCE
—VS—
GATE-SOURCE VOLTAGE



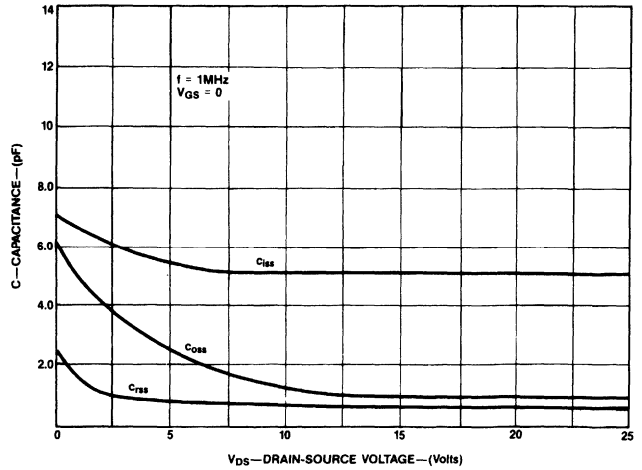
FORWARD TRANSCONDUCTANCE
—VS—
ON DRAIN CURRENT



ON DRAIN CURRENT
—VS—
GATE-SOURCE VOLTAGE



CAPACITANCES
—VS—
DRAIN-SOURCE VOLTAGE



N-CHANNEL ENHANCEMENT-MODE HIGH-VOLTAGE D-MOS FETs

ORDERING INFORMATION



FEATURES

- Low Capacitance (C_{oss} 1.0 pF typ.)
- Low Leakage (I_{pss} 0.5nA typ. @ 180V)
- High Gate Standoff Voltage ($\pm 100V$ min.)

APPLICATIONS

- Display Drivers
- AC-DC Relays
- Reed Relays
- Low-Power, High-Voltage Drivers

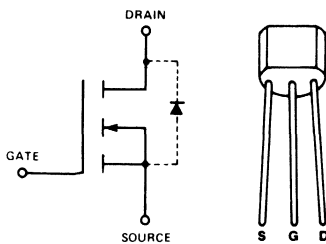
ABSOLUTE MAXIMUM RATINGS (T = +25°C unless otherwise noted.)

Drain-Source Voltage	200V
Drain-Gate Voltage ($V_{GS} = 0$)	200V
Gate-Source Voltage	$\pm 100V$
Continuous Drain Current (Note 1)	20mA
Peak Drain Current (Note 1)	40mA
Continuous Device Dissipation (Note 1)	300mW
Linear Derating Factor (Note 1)	2.4mW/°C

Operating Junction and Storage	
Temperature Range	-55 to +150°C
Storage Temperature Range	-55 to +150°C
Lead Temperature (1/16" from mounting surface for 30 Sec)	+260°C

Note 1: Not applicable to chips. Final value depends upon mounting substrate.

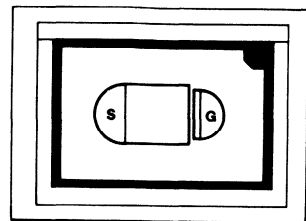
SCHEMATIC DIAGRAM



PACKAGE DIMENSIONS (TO-92) TO-226AA

(See Package 5)

CHIP CONFIGURATION



Drain is backside contact.
Dimensions: .025 × .035 × .020 inches

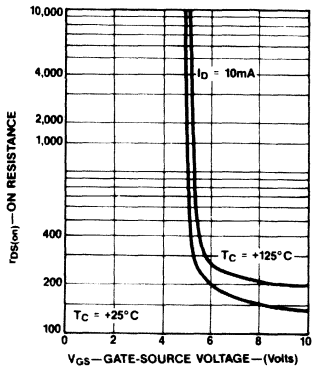
ELECTRICAL CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC		SD1202			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
1	BV_{DSS}	Drain Source Breakdown Voltage	200	260		V	$I_D = 1.0\mu\text{A}, V_{GS} = 0$	
2	I_{GSSF}	Gate Forward Leakage Current		.02	10	nA	$V_{GS} = 100\text{V}$	$V_{DS} = 0$
3	I_{GSSR}	Gate Reverse Leakage Current		-.02	-10		$V_{GS} = -100\text{V}$	
4	i_{DSS}	Drain-Source OFF Leakage Current		0.5	3.0		$V_{DS} = 180\text{V}$ $V_{GS} = 0$	
5					300			
6	$V_{GS(th)}$	Gate Source Threshold Voltage	1.0	4.0	5.0	V	$I_D = 10\mu\text{A}, V_{DS} = V_{GS}$	
7	$I_{D(on)}$	Drain-Source ON Current	40	55		mA	$V_{DS} = 25\text{V}, V_{GS} = 10\text{V}$	
8	$r_{DS(on)}$	Drain-Source ON Resistance		150	250	ohms	$V_{GS} = 10\text{V}$ $I_D = 10\text{mA}$	$T_C = +125^\circ\text{C}$
9					425			
10	g_{fs}	Common-Source Forward Transconductance	10	13		mS	$V_{DS} = 25\text{V}, I_D = 20\text{mA}$ $f = 1\text{KHz}$ (Note 1)	
11	C_{iss}	Common-Source Input Capacitance		5.0	10	pF	$V_{DS} = 25\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$	
12	C_{rss}	Common-Source Reverse Transfer Capacitance		0.8	1.0			
13	C_{oss}	Common-Source Output Capacitance		1.0	2.0			

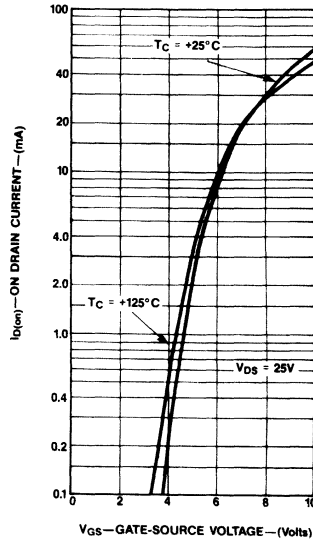
Note 1: Pulse Test 80 μ Sec, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise specified)

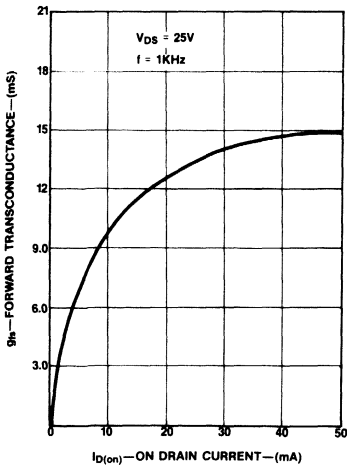
ON RESISTANCE
—VS—
GATE-SOURCE VOLTAGE



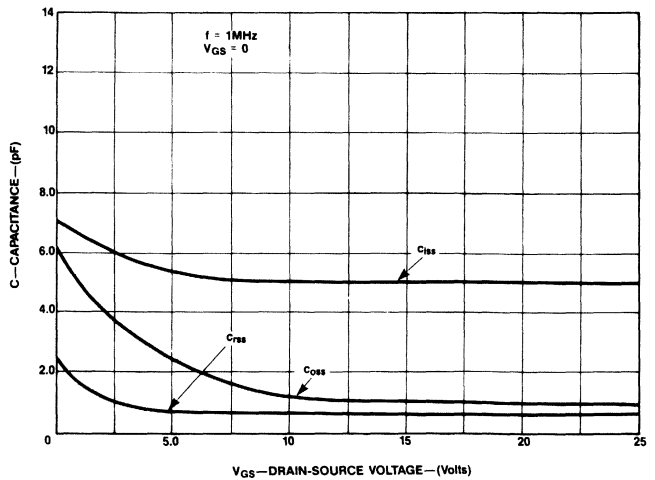
ON DRAIN CURRENT
—VS—
GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE
—VS—
ON DRAIN CURRENT



CAPACITANCES
—VS—
DRAIN-SOURCE VOLTAGE



N-CHANNEL ENHANCEMENT-MODE D-MOS FET SWITCHES

ORDERING INFORMATION

TO-92 Plastic Package	SD1500BD	SD1501BD
Sorted Chips in Wafer Pack	SD1500CHP	SD1501CHP
SOT-89 Surface Mount Pkg.	SD1500CY	SD1501CY
Description	600V, 60ohm	550V, 60ohm

FEATURES

- Guaranteed BVDS of 600V min
- Low Output and Transfer Capacitance
- Extended Safe Operating Area
- Available in Low Cost TO-92 Package
- Available in Surface Mount Package

APPLICATIONS

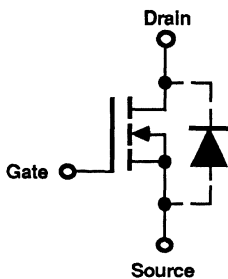
- Output Switching
- High Speed Pulse Amplifiers
- Solid-State Relays
- Display Drivers
- High Voltage ATE
- Telecommunications Switching

ABSOLUTE MAXIMUM RATINGS ($T_c = +25^\circ\text{C}$ unless otherwise noted)

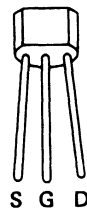
Drain-Source Voltage			
SD1500	600V		
SD1501	550V		
Drain-Gate Voltage ($V_{GS} = 0$)			
SD1500	600V		
SD1501	550V		
Gate-Source Voltage			
	$\pm 40V$		
Continuous Drain Current	$T_c = +25^\circ\text{C}$	$T_c = +100^\circ\text{C}$	
SD1500-01BD	180	65	mA
SD1500-01CY	115	55	mA

Peak Pulsed Drain Current			200mA
Continuous Device Dissipation			
	$T_c = +25^\circ\text{C}$	$T_c = +100^\circ\text{C}$	
SD1500-01BD	3.0	0.4	W
SD1500-01CY	1.2	0.3	W
Linear Derating Factor			
	$T_c = +25^\circ\text{C}$	$T_c = +100^\circ\text{C}$	
SD1500-01BD	24	3.0	mW/ $^\circ\text{C}$
SD1500-01CY	9.6	2.3	mW/ $^\circ\text{C}$
Operating Junction and Storage			
Temperature Range			-55 to +125 $^\circ\text{C}$
Lead Temperature (1/16" from mounting			
surface for 30 Sec)			+260 $^\circ\text{C}$

CONFIGURATION

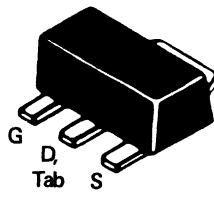


TO-226AA (TO-92)



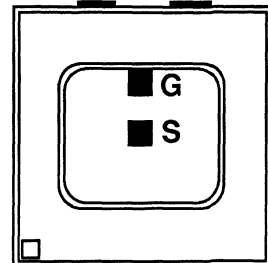
See Package 5

TO-243AA (SOT-89)



See Package 23

CHIP CONFIGURATION



Dimensions: 0.058 x 0.056 x 0.020 inches
Drain is backside contact.

ELECTRICAL CHARACTERISTICS ($T_c = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTICS		SD1500			SD1501			UNIT	TEST CONDITION	
			MIN	TYP	MAX	MIN	TYP	MAX			
1	BV _{DSS}	Drain-Source Breakdown Voltage	600	700		550	600		V	$I_D = 10\mu\text{A}, V_{GS} = 0$	
2		V _{GS(th)}	Gate-Source Threshold Voltage	1.0	2.1	4.0	1.0	2.1		4.0	$V_{DS} = V_{GS}, I_D = 1\text{mA}$
3	STATIC	I _{GSS}	Gate-Body Leakage Current		0.3	10		0.3	10	nA	$V_{GS} = 20\text{V}$ $V_{DS} = 0$
4											$T_c = +125^\circ\text{C}$
5		I _{DSS}	Drain-Source OFF Leakage Current			1.0				μA	$V_{DS} = 480\text{V}$ $V_{GS} = 0$
6						50					$T_c = +125^\circ\text{C}$
7									1.0		$V_{DS} = 440\text{V}$ $V_{GS} = 0$
8									50		$T_c = +125^\circ\text{C}$
9		I _{D(on)}	ON Drain Current (1)	100	260		100	260		mA	$V_{DS} = 25\text{V}, V_{GS} = 10\text{V}$
10		r _{DS(on)}	Drain-Source ON Resistance(1)		45	60		45	60		ohms
11					100			100		$T_c = +125^\circ\text{C}$	
12	g _{fs}	Common-Source(1) Forward Transcond.	100	215		100	215		mS	$V_{DS} = 25\text{V}, I_D = 100\text{mA}$ $f = 1\text{KHz}$ (Note 1)	
13	c _{iss}	Common-Source Input Capacitance		80	100		80	100		pF	$V_{DS} = 25\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$
14	c _{iss}	Common-Source Reverse Transfer Capacitance		1.0	2.0		1.0	2.0			
15	c _{oss}	Common-Source Output Capacitance		6.0	10		6.0	10			
16	t _{on}	Turn-On Time		7.0	12		7.0	12	nSec	$V_{DD} = 25\text{V}$ $R_L = 51\text{ ohms}$ $R_G = 51\text{ ohms}$ $V_{G(on)} = 10\text{V}$	
17	t _{off}	Turn-Off Time		7.0	12		7.0	12			

Note 1: Pulse Test 80 μSec , 1% Duty Cycle

SWITCHING TIMES TEST CIRCUIT

Input Pulse

$t_r \leq 0.5nSEC$

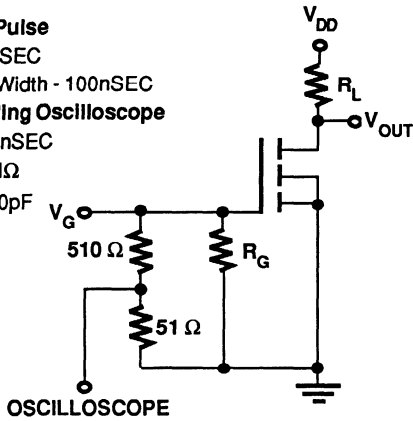
Pulse Width - 100nSEC

Sampling Oscilloscope

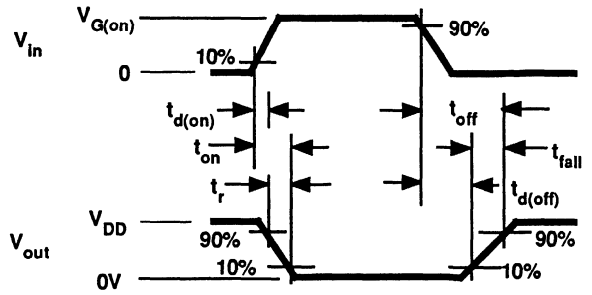
$t_r < 0.36nSEC$

$R_{in} > 1M\Omega$

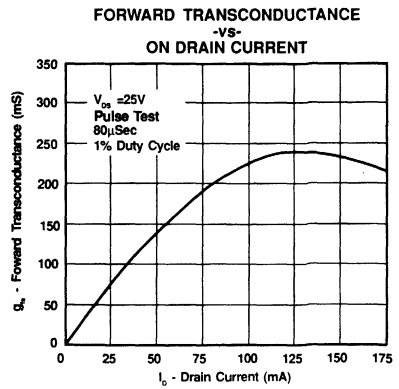
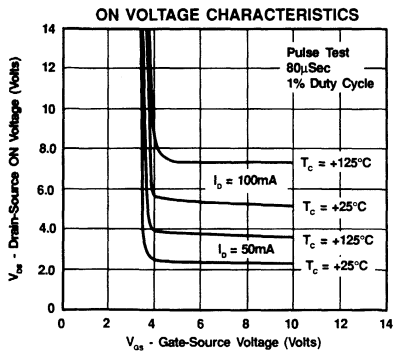
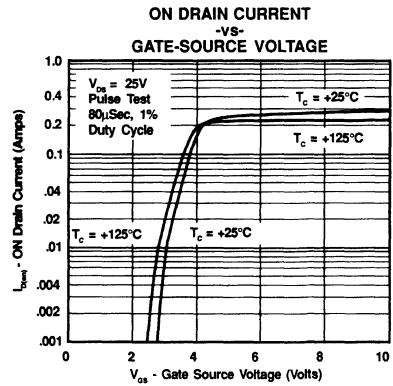
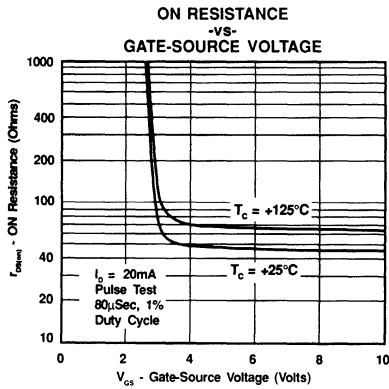
$C_{in} < 2.0pF$



TEST WAVEFORMS



TYPICAL PERFORMANCE CHARACTERISTICS ($T_c = +25^\circ C$ unless otherwise noted)



N-CHANNEL DEPLETION-MODE D-MOS FET

ORDERING INFORMATION



FEATURES

- Normally ON Configuration
- Low Interelectrode Capacitances
- High-Speed Switching
- Pin and Function Compatible to Industry Standard J-FETs with addition of Substrate Bias Pin.

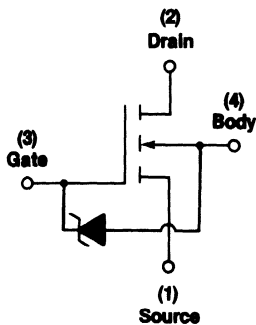
APPLICATIONS

- High-Speed Analog Switches
- Wide-Band RF Amplifiers
- Cascode Amplifiers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

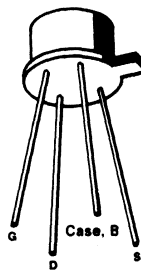
V _{DS} Drain-Source Voltage	+20V	I _D Continuous Drain Current	+50 mA
V _{SD} Source-Drain Voltage	+10V	P _D Total Device Dissipation	360 mW
V _{DB} Drain-Body Voltage	+25V	Derating Factor	2.88 mW/°C
V _{SB} Source-Body Voltage	+15V	T _J Operating Junction	
V _{GD} Gate-Drain Voltage	+25V	Temperature Range	-55 to +150°C
V _{GS} Gate-Source Voltage	+25V	T _S Storage Temperature Range	-55 to +150°C
V _{GB} Gate-Body Voltage	+25V	T _L Lead Temperature (1/16" from mounting surface for 10 sec.)	+260°C

SCHEMATIC DIAGRAM



Body internally connected to Case.

PIN CONFIGURATION



PACKAGE DIMENSIONS (TO-72) TO-206AF

(See Package 3)

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS							
1	STATIC	BV _{DS} Drain-Source Breakdown Voltage	20			V	I _D = 10 nA, V _{GS} = V _{BS} = -5V							
2		BV _{SD} Source-Drain Breakdown Voltage	10				I _S = 10 nA, V _{GD} = V _{BD} = -5V							
3		BV _{DB} Drain-Body Breakdown Voltage	25				I _D = 10 nA, V _{GB} = 0 Source Open							
4		BV _{SB} Source-Body Breakdown Voltage	15				I _S = 10 μA, V _{GB} = 0 Drain open							
5		I _{GSS(fwd)} Forward Gate Leakage Current			1.0	nA	V _{GS} = 25V, V _{DS} = V _{BS} = 0							
6		I _G Gate Operating Current			-3.0	-100	pA	V _{DG} = 20V I _D = 5.0 mA	T _A = +125°C					
7					-0.7	-10	nA	V _{BS} = -5.6V						
8		V _{GS(off)} Gate-Source Cutoff Voltage	-1.0		-5.0	V	V _{DS} = 10V, I _D = 1.0 μA V _{BS} = -5.6V							
9		V _{GS(on)} Gate-Source ON Voltage	-0.3		-3.0		V _{DG} = 10V, I _D = 5mA, V _{BS} = -5.6V							
10		I _{DSX} Zero Gate Voltage ⁽¹⁾ Drain Current	7.0		40	mA	V _{DS} = 10V V _{GS} = 0							
11			5.0				V _{BS} = -5.6V T _A = +125°C							
12		r _{DS(ON)} Drain-Source ON Resistance		100	150	ohms	I _D = 1.0mA, V _{GS} = 0, V _{BS} = -5.6V							
13	DYNAMIC	g _{fs} Common-Source ⁽¹⁾ Forward Transconductance	5.0	7.5	10	mmhos	V _{DG} = 10V I _D = 5.0 mA V _{BS} = -5.6V	f = 1 KHz						
14		g _{os} Common-Source Output Conductance		200	300	μmhos		pF	f = 1 MHz					
15		C _{iss} Common-Source Input Capacitance		3.5		pF	V _{DG} = 10V I _D = 5.0 mA V _{BS} = -5.6V			f = 1 MHz				
16		C _{oss} Common-Source Output Capacitance		1.2							pF	V _{DG} = 10V I _D = 5.0 mA V _{BS} = -5.6V	f = 1 MHz	
17		C _{rss} Common-Source Reverse Transfer Capacitance		0.3										pF
18		C _{i(gS + sb)} Source Node Capacitance		4.5				pF	V _{DG} = 10V I _D = 5.0 mA V _{BS} = -5.6V					

Note 1: Pulse Test, 80 μsec, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS: See TZ5911

P-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

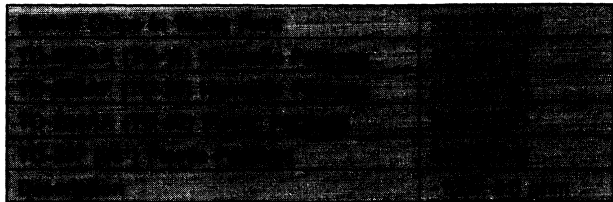
FEATURES

- Gate Stand-off Voltage, $\pm 40V$ min.
- Low Output and Transfer Capacitances
- Wide Variety of Packages
- N-Channel Complements Available

APPLICATIONS

- Complementary Voltage and Current Drivers
- Pulse Amplifiers
- Motor Controls
- Logic Interfaces

ORDERING INFORMATION



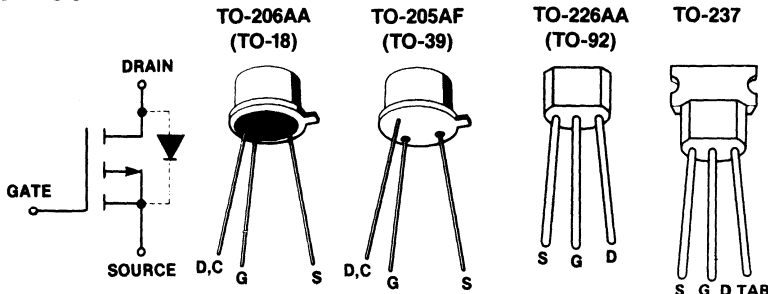
ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ C$ unless otherwise noted)

Drain-Source Voltage	-100V	
Drain-Gate Voltage ($V_{GS} = 0$)	-100V	
Gate-Source Voltage	$\pm 40V$	
Continuous Drain Current	$T_A = 25^\circ C$	$T_C = 25^\circ C$
SD2107AD	-26A	-43A
SD2107BD	-24A	-32A
SD2107DD	-26A	-43A
SD2107HD	-44A	-81A
Peak Pulsed Drain Current	-1.1A	

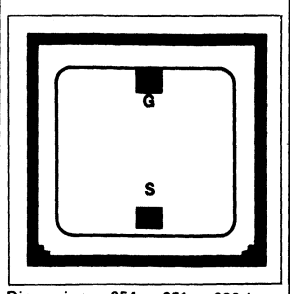
Continuous Device Dissipation	$T_A = +25^\circ C$	$T_C = +25^\circ C$	
	SD2107AD	0.36	1.8 W
	SD2107BD	0.3	1.0 W
	SD2107DD	0.36	1.8 W
	SD2107HD	1.0	6.25 W
Linear Derating Factor	$T_A = +25^\circ C$	$T_C = +25^\circ C$	
	SD2107AD	2.88	14.4 mW/ $^\circ C$
	SD2107BD	2.4	8.0 mW/ $^\circ C$
	SD2107DD	2.88	14.4 mW/ $^\circ C$
	SD2107HD	8.0	50 mW/ $^\circ C$

Operating Junction Temperature Range -55 to +150°C
 Storage Temperature Range -55 to +150°C
 Lead Temperature (1/16" from mounting surface for 30 Sec) +260°C

PIN CONFIGURATIONS



CHIP CONFIGURATION

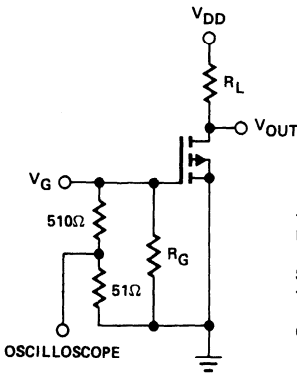


ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC	SD2107			UNIT	TEST CONDITIONS	
		MIN	TYP	MAX			
1	BV _{DSS} Drain-Source Breakdown Voltage	-100	-120		V	I _D = -10μA	V _{GS} = 0
2		-100	-120			I _D = -1.0mA	
3	I _{DSS} Drain-Source OFF Leakage Current			-100	nA	V _{DS} = -80V	T _A = +125°C
4				-5.0		V _{GS} = 0	
5	I _{GSS} Gate-Body Leakage Current			±10	nA	V _{GS} = ±30V	V _{DS} = 0
6				±1.0		V _{GS} = ±40V	
7	V _{GS(th)} Gate-Source Threshold Voltage	-1.5		-3.5	V	V _{DS} = V _{GS} , I _D = -1.0mA	
8	r _{DS(on)} Drain-Source (1) ON Resistance			15	ohms	V _{GS} = -5V, I _D = -0.1A	T _A = +125°C
9			3.9	5.0		V _{GS} = -10V, I _D = -0.5A	
10				8.0			
11	I _{D(on)} ON Drain Current (1)	-1.1			A	V _{DS} = -25V, V _{GS} = -10V	
12	g _{fs} Common-Source (1) Forward Transcond.	200	260		mmhos	V _{DS} = -25V, I _D = -0.5A f = 1KHz	
13	C _{iss} Common-Source Input Capacitance		60	80	pF	V _{DS} = -25V, V _{GS} = 0 f = 1MHz	
14	C _{rss} Common-Source Reverse Transfer Capacitance		5.0	8.0			
15	C _{oss} Common-Source Output Capacitance		10.5	20			
16	t _{on} Turn-On Time			16	nSec	V _{DD} = -25V R _L = 51 ohms R _G = 51 ohms V _{G(on)} = -10V	
17	t _{off} Turn-Off Time			16			

Note 1: Pulse Test, 80μ Sec, 1% Duty Cycle

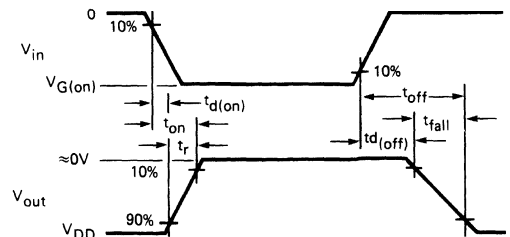
SWITCHING TIME TEST CIRCUIT



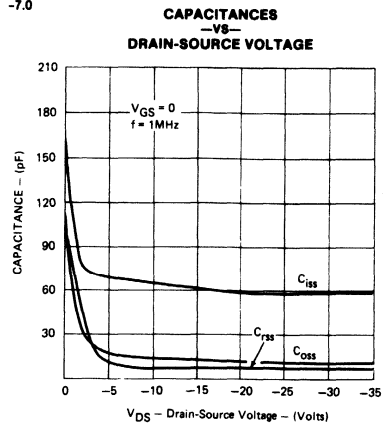
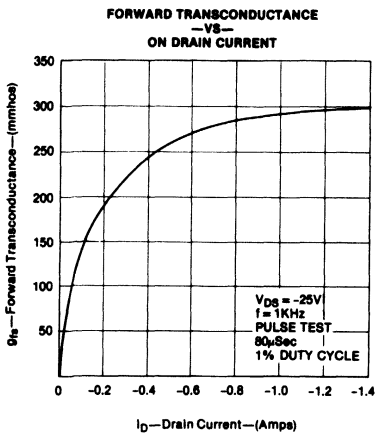
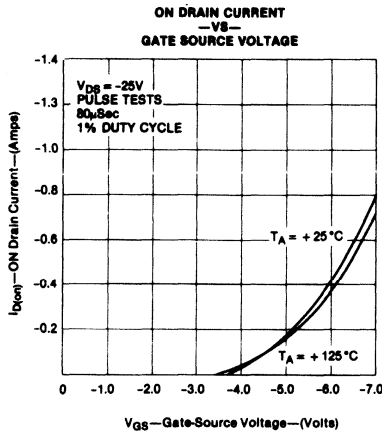
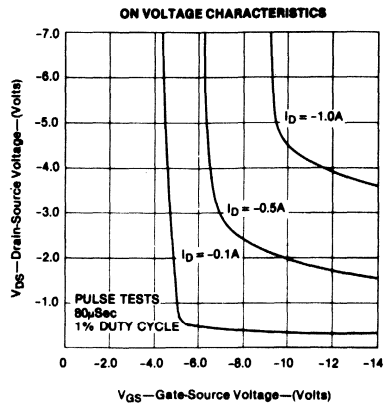
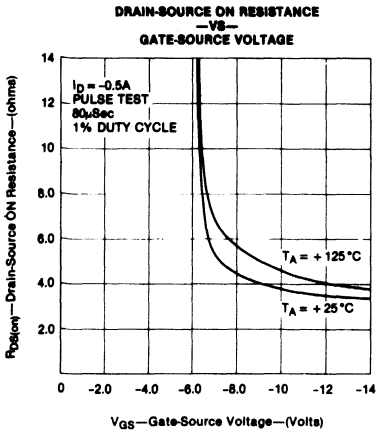
INPUT PULSE
t_r < 0.5 nSEC
PULSE WIDTH - 100 nSEC

SAMPLING OSCILLOSCOPE
t_r < 0.36 nSEC
R_{in} > 1 MΩ
C_{in} < 2.0 pF

TEST WAVEFORMS



TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)



N-CHANNEL DEPLETION-MODE D-MOS FET

ORDERING INFORMATION

TO-206AF (TO-72) Hermetic Package	SD2200DE
with Shorting Ring on leads	SD2200DEA
Description	20V, 750

FEATURES

- Normally ON Configuration
- Low Interelectrode Capacitances
- High-Speed Switching
- Pin and Function Compatible to Industry Standard J-FETs with addition of Substrate Bias Pin

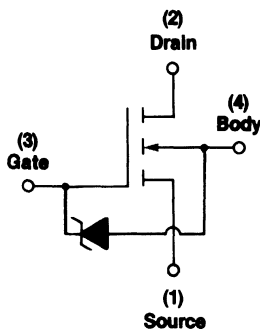
APPLICATIONS

- High-Speed Analog Switches
- Wide-Band RF Amplifiers
- Cascode Amplifiers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

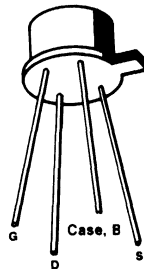
V _{DS} Drain-Source Voltage	+20V	I _D Continuous Drain Current	+100 mA
V _{SD} Source-Drain Voltage	+10V	P _D Total Device Dissipation	360 mW
V _{DB} Drain-Body Voltage	+25V	Derating Factor	2.88 mW/°C
V _{SB} Source-Body Voltage	+15V	T _J Operating Junction Temperature Range	-55 to +150°C
V _{GD} Gate-Drain Voltage	+25V	T _S Storage Temperature Range	-55 to +150°C
V _{GS} Gate-Source Voltage	+25V	T _L Lead Temperature (1/16" from mounting surface for 10 sec.)	+260°C
V _{GB} Gate-Body Voltage	+25V		

SCHEMATIC DIAGRAM



Body internally connected to Case

PIN CONFIGURATION



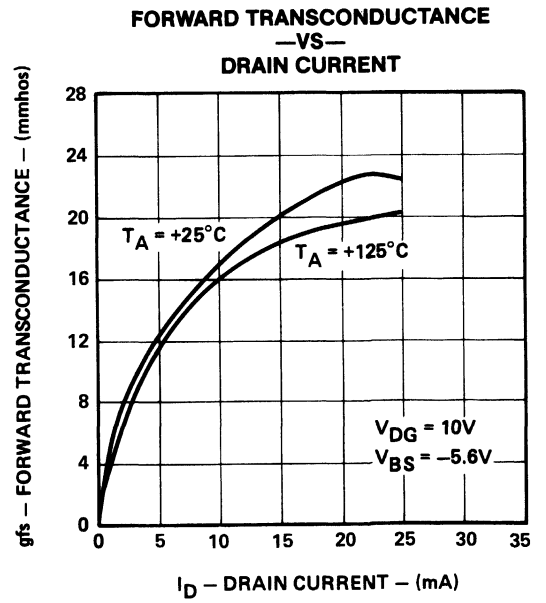
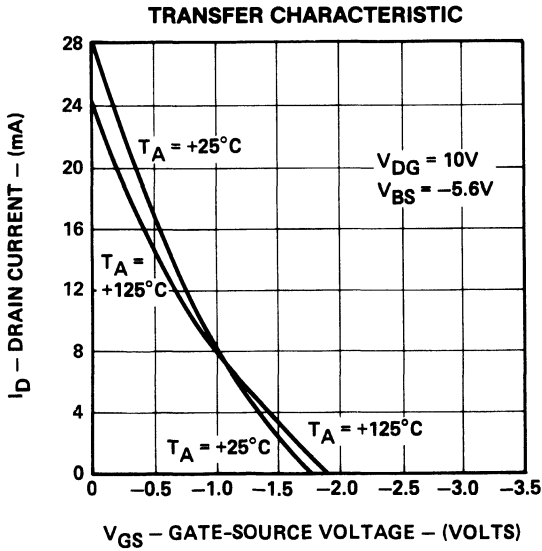
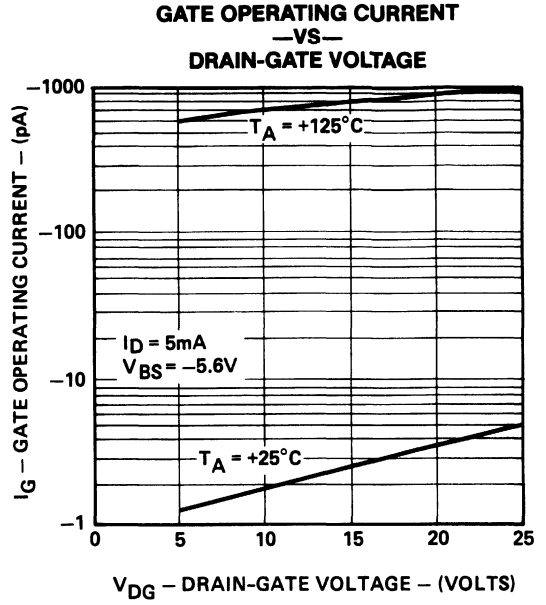
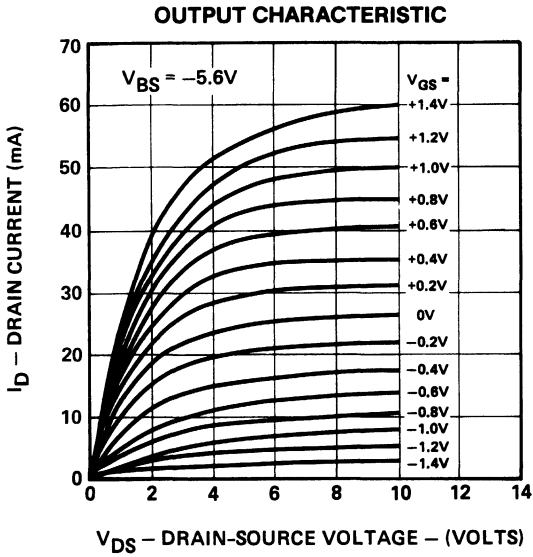
PACKAGE DIMENSIONS (TO-72) TO-206AF (See Package 3)

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$, per side, unless otherwise noted)

#	CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
1	STATIC	BV_{DS} Drain-Source Breakdown Voltage	20			V	$I_D = 20\text{ nA}$, $V_{GS} = V_{BS} = -5\text{V}$	
2		BV_{SD} Source-Drain Breakdown Voltage	10				$I_S = 20\text{ nA}$, $V_{GD} = V_{BD} = -5\text{V}$	
3		BV_{DB} Drain-Body Breakdown Voltage	25				$I_D = 20\text{ nA}$, $V_{GB} = 0$ Source Open	
4		BV_{SB} Source-Body Breakdown Voltage	15				$I_S = 10\text{ }\mu\text{A}$, $V_{GB} = 0$ Drain open	
5		$I_{GSS(fwd)}$ Forward Gate Leakage Current			2.0	nA	$V_{GS} = 25\text{V}$, $V_{DS} = V_{BS} = 0$	
6		I_G Gate Operating Current		-6.0	-100	pA	$V_{DG} = 20\text{V}$ $I_D = 5.0\text{ mA}$ $V_{BS} = -5.6\text{V}$	$T_A = +125^\circ\text{C}$
7				-1.4	-10	nA		
8		$V_{GS(off)}$ Gate-Source Cutoff Voltage	-1.0		-5.0	V	$V_{DS} = 10\text{V}$, $I_D = 2.0\text{ }\mu\text{A}$ $V_{BS} = -5.6\text{V}$	
9		$V_{GS(on)}$ Gate-Source ⁽¹⁾ ON Voltage	-0.3		-3.0		$V_{DG} = 10\text{V}$, $I_D = 10\text{mA}$, $V_{BS} = -5.6\text{V}$	
10		I_{DSX} Zero Gate Voltage ⁽¹⁾ Drain Current	14		60	mA	$V_{DS} = 10\text{V}$ $V_{GS} = 0$ $V_{BS} = -5.6\text{V}$	$T_A = +125^\circ\text{C}$
11			10					
12		$r_{DS(on)}$ Drain-Source ON Resistance		50	75	ohms	$I_D = 1.0\text{mA}$, $V_{GS} = 0$, $V_{BS} = -5.6\text{V}$	
13	DYNAMIC	g_{fs} Common-Source ⁽¹⁾ Forward Transconductance	10	15	20	mmhos	$V_{DG} = 10\text{V}$ $I_D = 10\text{ mA}$ $V_{BS} = -5.6\text{V}$	f = 1 KHz
14		g_{os} Common-Source Output Conductance		380	600	μmhos		pF
15		C_{iss} Common-Source Input Capacitance		7.0				
16		C_{oss} Common-Source Output Capacitance		2.4				
17		C_{rss} Common-Source Reverse Transfer Capacitance		0.6				
18		$C_{(gs + sb)}$ Source Node Capacitance		9.0				

Note 1: Pulse Test, 80 μsec , 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)



P-CHANNEL ENHANCEMENT MODE D-MOS FET

ORDERING INFORMATION



FEATURES

- Ultra-Low Channel OFF Leakage, <math>< 500\text{pA}</math>
- Low Interelectrode Capacitances
- N-Channel Complements available, SD1201
- Gate Standoff Voltage, $\pm 40\text{V min.}$

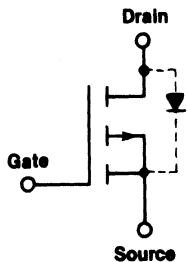
APPLICATIONS

- High-Voltage Drivers
- High-Voltage Level Translators
- Reed Relay Replacements

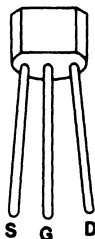
ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$, unless otherwise specified)

Drain-Source Voltage	-400V	Continuous Drain Current	$T_A = +25^\circ\text{C}$ -15mA	$T_C = +25^\circ\text{C}$ -25mA
Drain-Gate Voltage	-400V			
Gate-Source Voltage	$\pm 40\text{V}$			
Operating and Storage Temperature Range	-55 to $+125^\circ\text{C}$	Continuous Device Dissipation	$T_A = +25^\circ\text{C}$ 0.30W	$T_C = +25^\circ\text{C}$ 1.0W
Lead Temperature (1/16" from mounting Surface for 10 sec.)	$+260^\circ\text{C}$	Linear Derating Factor	$T_A = +25^\circ\text{C}$ 3.0mW/ $^\circ\text{C}$	$T_C = +25^\circ\text{C}$ 10mW/ $^\circ\text{C}$

PIN CONFIGURATION

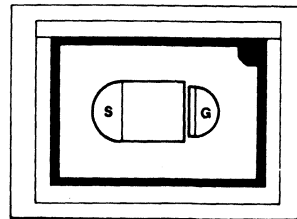


TO-226AA
(TO-92)



(See Package 5)

CHIP CONFIGURATION

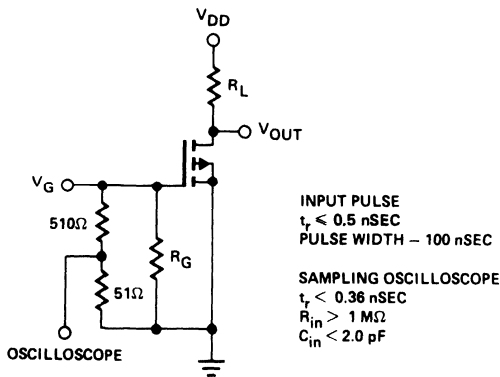


Dimensions: .025 x .035 x .020 in.
Drain is backside contact.

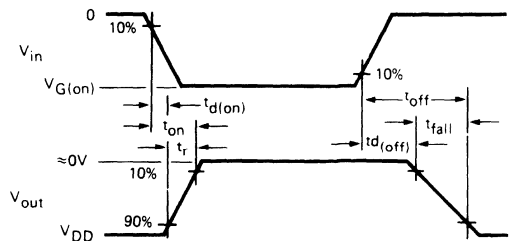
ELECTRICAL CHARACTERISTICS (T_A = +25°C per channel, unless otherwise noted)

#	CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITIONS
1	STATIC	BV _{DSS} Drain-Source Breakdown Voltage	-400			V	I _D = -100μA, V _{GS} = 0 I _D = -1.0μA
2			-400				
3		I _{DSS} Drain-Source OFF Leakage Current		-80	-500	pA	V _{DS} = -100V, V _{GS} = 0
4		I _{GBS} Gate-Body Leakage Current			±1.0	nA	V _{GB} = ±20V, V _{DS} = 0
5		V _{GS(th)} Gate-Source Threshold Voltage	-2.0		-5.0	V	V _{DS} = V _{GS} , I _D = -0.5mA
7		r _{DS(on)} Drain-Source ON Resistance		500	700	ohms	I _D = -10mA, V _{GS} = -10V
8		I _{D(on)} Drain-Source ON Current	-15	-40		mA	V _{DS} = -25V, V _{GS} = -10V
9		DYNAMIC	g _{fs} Common-Source Forward Transconductance	3.0	7.5		mmhos
10	C _{iss} Common-Source Input Capacitance			8.0	10	pF	V _{DS} = -25V, V _{GS} = 0, f = 1MHz
11	C _{oss} Common-Source Output Capacitance			1.5	2.0		
12	Common-Source Reverse Transfer Capacitance			0.8	1.0		
13	t _{d(on)} Turn-ON Delay Time			6		nS	V _{DD} = -25V, V _{G(on)} = -10V R _L = 500Ω R _G = 51Ω
14	t _r Rise time			6			
15	t _{d(off)} Turn-OFF Delay Time			8			
16	t _f Fall Time			6			

SWITCHING TIME TEST CIRCUIT

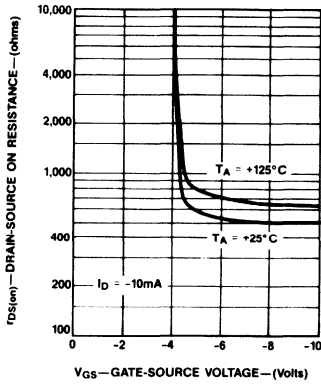


TEST WAVEFORMS

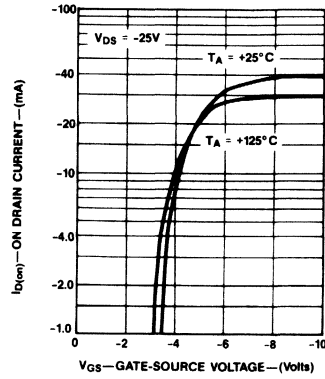


TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ per channel, unless otherwise noted)

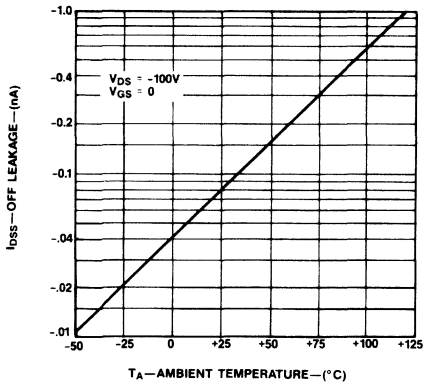
DRAIN-SOURCE ON RESISTANCE
—vs—
GATE-SOURCE VOLTAGE



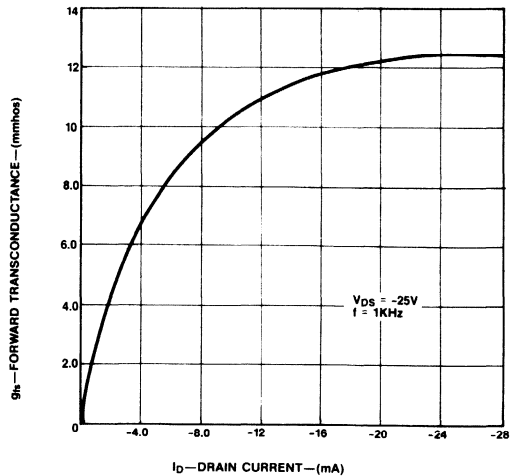
ON DRAIN CURRENT
—vs—
GATE-SOURCE VOLTAGE



DRAIN-SOURCE OFF LEAKAGE CURRENT
—vs—
AMBIENT TEMPERATURE



FORWARD TRANSCONDUCTANCE
—vs—
ON DRAIN CURRENT



N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION

Sorted Chips in Wafer Pack	SD3300CHP	SD3301CHP
TO-205AF (TO-39) Hermetic Package	SD3300HD	SD3301HD
TO-226AA (TO-92) Plastic Package	SD3300BD	SD3301BD
TO-237 (TO-92*) Plastic Package	SD3300AD	SD3301AD
Description	100V, 0.8 ohm	80V, 0.4 ohm

FEATURES

- Gate Stand-off Voltage, $\pm 40V$ min.
- Continuous I_D of 1 Amp in small package
- Wide Variety of Packages

APPLICATIONS

- Motor Controls
- Line Drivers
- Power Supplies

ABSOLUTE MAXIMUM RATINGS ($T_C = +25^\circ C$ unless otherwise noted)

Drain-Source Voltage

SD3300	100V
SD3301	60V

Drain-Gate Voltage ($R_{GS} = 1M\Omega$)

SD3300	100V
SD3301	60V

Gate-Source Voltage

Continuous Drain Current

	$T_C = +100^\circ C$	$T_C = +25^\circ C$
SD3300AD	1.2A	1.9A
SD3300BD	1.0A	1.6A
SD3300HD	2.25A	3.5A
SD3301AD	1.4A	2.3A
SD3301BD	1.2A	1.9A
SD3301HD	2.7A	4.3A

Peak Pulsed Drain Current 8.0A

Maximum Power Dissipation

	$T_C = +100^\circ C$	$T_C = +25^\circ C$
HD, TO-39 Pkg.	6.0W	15W
BD, TO-92 Pkg.	1.2W	3.0W
AD, TO-237 Pkg.	1.7W	4.3W

Linear Derating Factor

	Junction to Ambient ($mW/^\circ C$)	Junction to Case ($mW/^\circ C$)
HD, TO-39 Pkg.	8.0	120
BD, TO-92 Pkg.	3.2	24
AD, TO-237 Pkg.	4.8	34.4

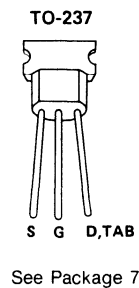
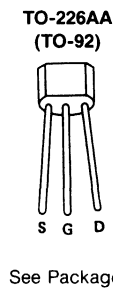
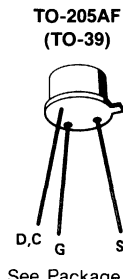
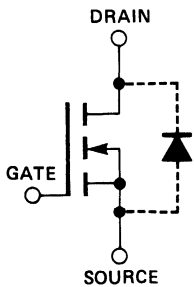
Operating Junction and Storage

Temperature Range -55 to $+150^\circ C$

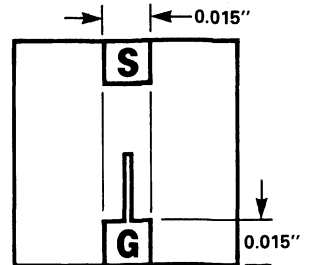
Lead Temperature (1/16" from mounting

surface for 30 Sec) $+260^\circ C$

PIN CONFIGURATIONS



CHIP CONFIGURATION



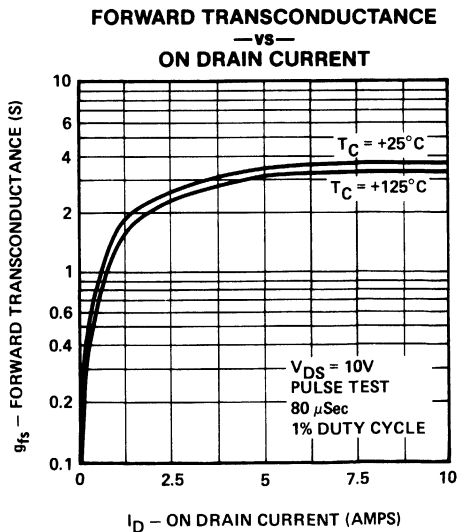
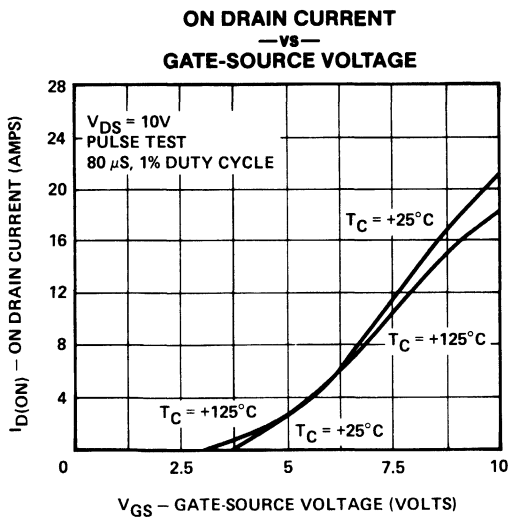
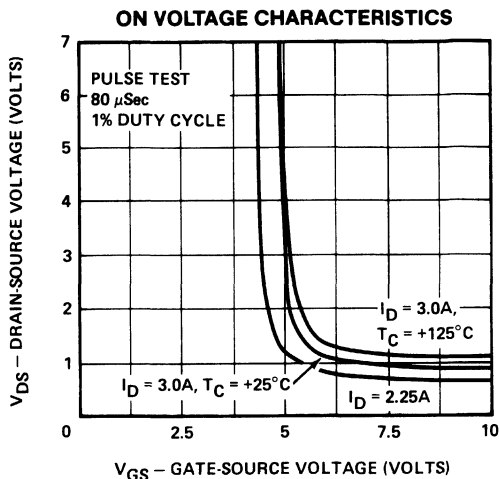
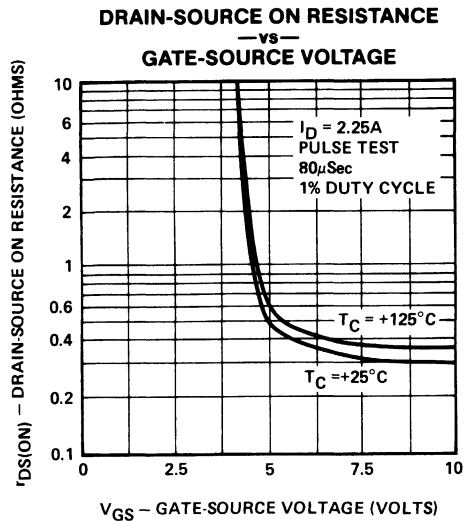
Dimensions: .078x.078x.020 in.
Drain is backside contact.

ELECTRICAL CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC	SD3300			SD3301			UNIT	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX			
1	BV_{DSS} Drain-Source Breakdown Voltage	100	125		60	90		V	$I_D = 250\mu\text{A}, V_{GS} = 0$	
2	$V_{GS(th)}$ Gate-Source Threshold Voltage	1.0		3.0	1.0		3.0	V	$V_{DS} = V_{GS}$ $I_D = 250\mu\text{A}$	
3		0.4			0.4					$T_C = +125^\circ\text{C}$
4	I_{GAS} Gate-Body Leakage Current			100			100	nA	$V_{GS} = 20\text{V}, V_{DS} = 0$	
5				200			200			$T_C = +125^\circ\text{C}$
6				-100			-100			$V_{GS} = -20\text{V}, V_{DS} = 0$
7	I_{DSS} Drain-Source OFF Leakage Current			1.0				μA	$V_{DS} = 80\text{V}, V_{GS} = 0$	
8				1000						$T_C = +125^\circ\text{C}$
9							1.0			$V_{DS} = 48\text{V}, V_{GS} = 0$
10							1000			$T_C = +125^\circ\text{C}$
11	$I_{D(on)}$ ON Drain Current ⁽¹⁾	3.0			3.5			A	$V_{DS} = 10\text{V}, V_{GS} = 10\text{V}$	
12	$V_{DS(on)}$ Drain-Source ⁽¹⁾ ON Voltage			1.8				V	$V_{GS} = 10\text{V}, I_D = 3.0\text{A}$	
13							1.4		$V_{GS} = 10\text{V}, I_D = 3.5\text{A}$	
14	$r_{DS(on)}$ Drain-Source ⁽¹⁾ ON Resistance			0.6			0.4	ohms	$V_{GS} = 10\text{V}$	
15				1.08			0.72		$I_D = 2.25\text{A}$ $T_C = +125^\circ\text{C}$	
16	g_{fs} Common-Source ⁽¹⁾ Forward Transcond.	1.0		3.0	1.0		3.0	S(U)	$V_{DS} = 10\text{V}$ $I_D = 2.25\text{A}$ $f = 1\text{KHz}$	
17	C_{iss} Common-Source Input Capacitance			200			200	pF	$V_{DS} = 25\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$	
18	C_{rss} Common-Source Reverse Transfer Capacitance			25			25			
19	C_{oss} Common-Source Output Capacitance			100			100			
20	$t_{d(on)}$ Turn-ON Delay Time			15			15	nsec	$V_{DD} = 34\text{V}$ $R_L = 15\text{ ohms}$ $R_G = 25\text{ ohms}$ $V_{GS(on)} = 10\text{V}$	
21	t_r Rise Time			25			25			
22	$t_{d(off)}$ Turn-OFF Delay Time			25			25			
23	t_f Fall Time			20			20			
24	I_S Continuous Source Current ⁽¹⁾	3.0			3.5			A		
25	I_{SM} Peak Source Current ⁽¹⁾	8.0			8.0					
26	V_{SD} Source-Drain ⁽¹⁾ Forward Voltage			2.0				V	$V_{GS} = 0$ $I_S = 3.0\text{A}$	
27							2.0		$I_S = 3.5\text{A}$	

Note 1: Pulse Test 80 μSec , 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)



N-CHANNEL ENHANCEMENT-MODE QUAD D-MOS FET ANALOG SWITCH ARRAYS

ORDERING INFORMATION



Note: Available in SO-14 surface mount package, refer to SD5400-02 series

FEATURES

- High Input to Output Isolation—120dB typical
- Low feedthrough and feedback transients
- Low Inter-electrode Capacitances

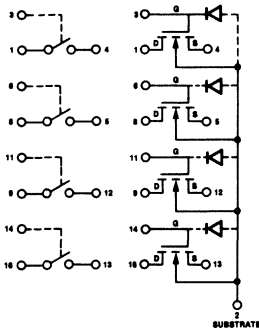
APPLICATIONS

- ±10V Analog Switches—SD5000
- ±7.5V Analog Switches—SD5002
- ±5V Analog Switches—SD5001
- Sample and Hold
- Wide-Band, Dual Differential Amplifiers

ABSOLUTE MAXIMUM RATINGS (per channel, T_A = +25°C unless otherwise noted)

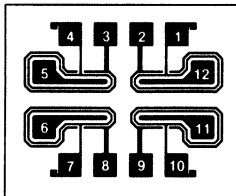
PARAMETER	SD5000	SD5001	SD5002	UNITS	
V _{DS}	+20	+10	+15	Vdc	I _D Continuous Drain Current 50mA
V _{SD}	+20	+10	+15	Vdc	P _D Total Package Power Dissipation (at or below T _A = +25°C) 640mW
V _{DB}	+25	+15	+22.5	Vdc	Linear Derating Factor 10.67mW/°C
V _{SB}	+25	+15	+22.5	Vdc	P _D Single Device Power Dissipation (at or below T _A = +25°C) 300mW
V _{GS}	-25	-15	-22.5	Vdc	T _j Operating Junction Temperature Range -55 to +85 °C
	+30	+25	+30	Vdc	T _S Storage Temperature Range . . -55 to +150 °C
V _{GB}	-0.3	-0.3	-0.3	Vdc	
	+30	+25	+30	Vdc	
V _{GD}	-25	-15	-22.5	Vdc	
	+30	+25	+30	Vdc	

SCHEMATIC DIAGRAM



Note: Pin numbers correspond to Package Pin-out

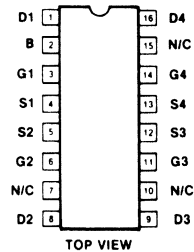
CHIP CONFIGURATION



PAD NO.	PAD FUNCTION	PAD NO.	PAD FUNCTION
1	Gate No. 1	7	Gate No. 3
2	Source No. 1	8	Source No. 3
3	Source No. 2	9	Source No. 4
4	Gate No. 2	10	Gate No. 4
5	Drain No. 2	11	Drain No. 4
6	Drain No. 3	12	Drain No. 1

Dimensions: .041 × .033 × .013 inches

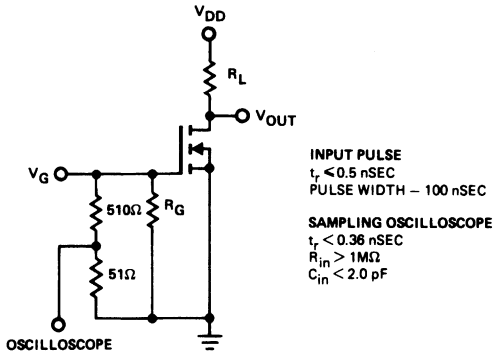
PIN CONFIGURATION



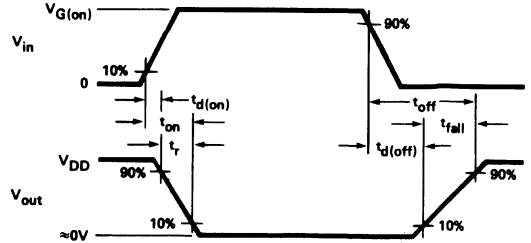
TOP VIEW

DIMENSIONS
16-Pin Plastic DIP
See Package 10
16-Pin Ceramic DIP
See Package 15

SWITCHING TIMES TEST CIRCUIT

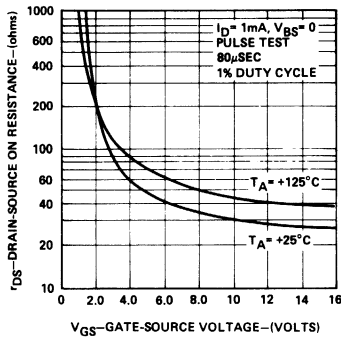


TEST WAVEFORMS

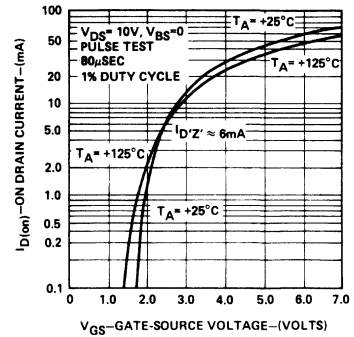


TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

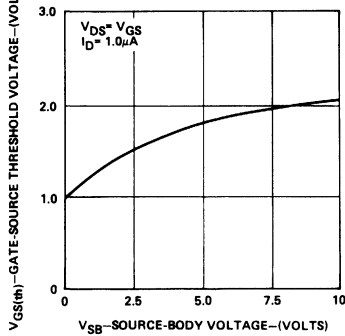
DRAIN-SOURCE ON RESISTANCE
—vs—
GATE-SOURCE VOLTAGE



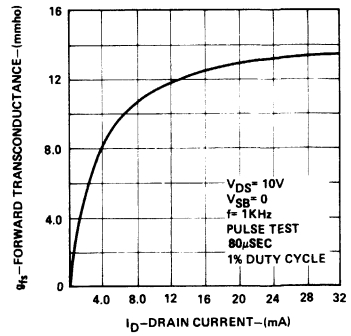
ON DRAIN CURRENT
—vs—
GATE-SOURCE VOLTAGE



GATE-SOURCE THRESHOLD VOLTAGE
—vs—
SOURCE-BODY VOLTAGE



FORWARD TRANSCONDUCTANCE
—vs—
ON DRAIN CURRENT



ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	PARAMETER	SD5000			SD5001			SD5002			UNIT	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
1	BV_{DS} Drain-Source Breakdown Voltage	20	25		10	25		15	25		V	$I_D = 10\text{nA}$ $V_{GS} = V_{BS} = -5\text{V}$
2	BV_{SD} Source-Drain Breakdown Voltage	20			10			15			V	$I_S = 10\text{nA}$ $V_{GD} = V_{BD} = -5\text{V}$
3	BV_{DB} Drain-Substrate Breakdown Voltage	25			15			22.5			V	$I_D = 10\text{nA}, V_{GB} = 0$ Source Open
4	BV_{SB} Source-Substrate Breakdown Voltage	25			15			22.5			V	$I_S = 10\mu\text{A}, V_{GB} = 0$ Drain Open
5	$I_{D(off)}$ Drain-Source Off Current						10				nA	$V_{DS} = 10\text{V}$
6									10		nA	$V_{DS} = 15\text{V}$
7				10							nA	$V_{DS} = 20\text{V}$
8	$I_{S(off)}$ Source-Drain OFF Current						10				nA	$V_{SD} = 10\text{V}$
9									10		nA	$V_{SD} = 15\text{V}$
10				10							nA	$V_{SD} = 20\text{V}$
11	I_{GBS} Gate-Body Leakage Current						1.0				μA	$V_{GB} = 25\text{V}$
12				1.0							μA	$V_{GB} = 30\text{V}$
13	$V_{GS(th)}$ Gate Threshold Voltage	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V	$V_{DS} = V_{GS}, I_D = 1\mu\text{A}$ $V_{SB} = 0$
14	$r_{DS(on)}$ Drain-Source ON Resistance		50	70		50	70		50	70	ohms	$V_{GS} = 5\text{V}$
15			30			30			30			$V_{GS} = 10\text{V}$
16			23			23			23			$V_{GS} = 15\text{V}$
17			19			19			19			$V_{GS} = 20\text{V}$
18	r_{DSM} ON Resistance Match		1.0	5.0		1.0	5.0		1.0	5.0		$V_{GS} = 5\text{V}$
19	g_{fs} Common-Source Forward Transcond.	10	12		10	12		10	12		mmhos	$V_{DS} = 10\text{V}, I_D = 20\text{mA}$ $f = 1\text{KHz}, V_{SB} = 0$
20	$C_{(gs + gd + gb)}$ Gate Node Capacitance		2.4	3.5		2.4	3.5		2.4	3.5	pF	$V_{DS} = 10\text{V}$ $V_{GS} = V_{BS} = -15\text{V}$ $f = 1\text{MHz}$
21	$C_{(gs + db)}$ Drain Node Capacitance		1.3	1.5		1.3	1.5		1.3	1.5		
22	$C_{(gs + sb)}$ Source Node Capacitance		3.5	4.0		3.5	4.0		3.5	4.0		
23	$C_{(dg)}$ Reverse Transfer Capacitance		0.3	0.5		0.3	0.5		0.3	0.5		
24	C_T Cross Talk		-107			-107			-107			
25	$t_{d(on)}$ Turn ON Delay Time		0.7	1.0		0.7	1.0		0.7	1.0	nSec	$V_{DD} = 5\text{V}, V_{G(on)} = 10\text{V}$ $R_L = 680\Omega, R_G = 51\Omega$
26	t_r Rise Time		0.8	1.0		0.8	1.0		0.8	1.0		
27	t_{off} Turn OFF Time		10			10			10			

N-CHANNEL ENHANCEMENT-MODE QUAD D-MOS FET ANALOG SWITCH ARRAYS

ORDERING INFORMATION

Sorted Chips in Wafer Pack	SD5100CHP	SD5101CHP
14-Pin Plastic Dual In-Line Package	SD5100N	SD5101N
Description	30V, 70 ohm	15V, 70 ohm

FEATURES

- Common source for 4 channels
- Low feedthrough and feedback transients
- Low Inter-electrode Capacitances

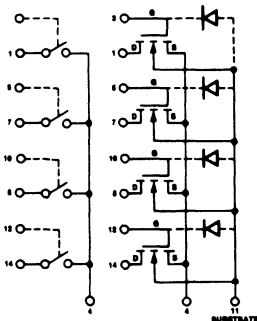
APPLICATIONS

- +30V Switch Drivers—SD5100
- +15V Switch Drivers—SD5101

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

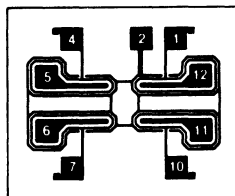
PARAMETER	SD5100	SD5101	UNITS	
V_{DS}	+30	+15	Vdc	I_D Continuous Drain Current 50mA
V_{SD}	+0.5	+0.5	Vdc	P_D Total Package Power Dissipation (at or below $T_A = +25^\circ\text{C}$) 640mW
V_{DB}	+30	+15	Vdc	Linear Derating Factor 10.67mW/ $^\circ\text{C}$
V_{SB}	+0.5	+0.5	Vdc	P_D Single Device Power Dissipation (at or below $T_A = +25^\circ\text{C}$) 300mW
V_{GS}	+20	+20	Vdc	T_J Operating Junction Temperature Range -55 to $+85^\circ\text{C}$
V_{GB}	+20	+20	Vdc	T_S Storage Temperature Range -55 to $+150^\circ\text{C}$
V_{GD}	-0.3	-0.3	Vdc	
	+20	+20	Vdc	
	-30	-15	Vdc	

SCHEMATIC DIAGRAM



Note: Pin numbers correspond to Package Pin-out

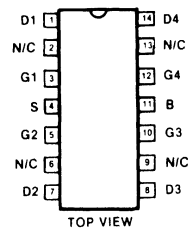
CHIP CONFIGURATION



PAD NO.	PAD FUNCTION	PAD NO.	PAD FUNCTION
1	Gate No. 1	7	Gate No. 3
2	Source	10	Gate No. 4
4	Gate No. 2	11	Drain No. 4
5	Drain No. 2	12	Drain No. 1
6	Drain No. 3		

Dimensions: .041 x .033 x .013 inches

PIN CONFIGURATION



DIMENSIONS
14-Pin Plastic DIP
See Package 9

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC		SD5100			SD5101			UNIT	TEST CONDITIONS	
			MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV _{DS} Drain-Source Breakdown Voltage	30	35		15	30		V	$I_D = 1.0\mu\text{A}, V_{GS} = V_{BS} = 0$	
2		BV _{SD} Source-Drain Breakdown Voltage	0.5			0.5			V	$I_S = 10\text{nA}, V_{GD} = V_{BD} = 0$	
3		BV _{DB} Drain-Substrate Breakdown Voltage	30			15			V	$I_D = 1.0\mu\text{A}, V_{GB} = 0$ Source Open	
4		BV _{SB} Source-Substrate Breakdown Voltage	0.5			0.5			V	$I_S = 100\text{nA}, V_{GB} = 0$ Drain Open	
5		I _{D(off)} Drain-Source OFF Current		1.0	10		1.0	10	nA	$V_{DS} = 10\text{V}, V_{GS} = V_{BS} = 0$	
6		I _{G(S)} Gate-Substrate Leakage Current			10			10	μA	$V_{GS} = 20\text{V}, V_{DB} = V_{SB} = 0$	
7		V _{GS(th)} Gate-Source Threshold Voltage	0.5	1.0	2.0	0.5	1.0	2.0	V	$I_D = 1.0\mu\text{A}, V_{DS} = V_{GS}$ $V_{SB} = 0$	
8		r _{DS(on)} Drain-Source ON Resistance			50	70		50	70	ohms	$V_{GS} = 5\text{V}$
9					30	45		30	45	ohms	$V_{GS} = 10\text{V}$
10					23			23		ohms	$V_{GS} = 15\text{V}$
11					19			19		ohms	$V_{GS} = 20\text{V}$
12		r _{DSM} ON Resistance Match		1.0	5.0		1.0	5.0	ohms	$V_{GS} = 5\text{V}$	I _D = 1mA V _{SB} = 0
13	g _{fs} Common-Source Forward Transcond	10	15		10	15		mmhos	$V_{DS} = 10\text{V}, I_D = 20\text{mA}$ $f = 1\text{KHz}, V_{SB} = 0$		
14	c _(gs+gd+gb) Gate Node Capacitance		2.4	3.5		2.4	3.5	pF	$V_{DS} = 10\text{V}$ $V_{GS} = V_{BS} = -5\text{V}$ $f = 1\text{MHZ}$		
15	c _(gd+db) Drain Node Capacitance		1.3	1.5		1.3	1.5				
16	c _{dg} Reverse Transfer Capacitance		0.3	0.5		0.3	0.5				
17	C _T Cross Talk		-107			-107				dB	$f = 3\text{KHz}, R_G = 600\Omega$

N-CHANNEL ENHANCEMENT-MODE QUAD D-MOS FET DRIVER ARRAY

ORDERING INFORMATION

Sorted Chips in 1000-Pin Pack	30V, 50mA
1000-Pin Plastic Dual In-Line Package	30V, 50mA
Description	30V, 50mA

FEATURES

- Normally OFF configuration
- Low Interelectrode capacitance
- High-speed switching

APPLICATIONS

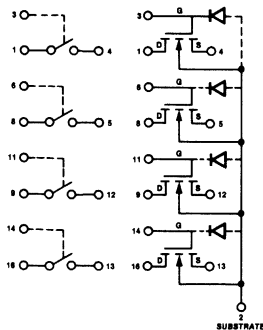
- +30V Analog Switch Drivers
- Wide-Band Dual Differential Amplifiers

ABSOLUTE MAXIMUM RATINGS (per channel, $T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DS} Drain-Source Voltage	+30Vdc
V_{SD} Source-Drain Voltage	+0.5Vdc
V_{DB} Drain-Body Voltage	+30Vdc
V_{SB} Source-Body Voltage	+15Vdc
V_{GS} Gate-Source Voltage	+25Vdc
V_{GB} Gate-Body Voltage	+25Vdc
Gate-Body Voltage	-0.3Vdc
V_{GD} Gate-Drain Voltage	+25Vdc
I_D Continuous Drain Current	50mA

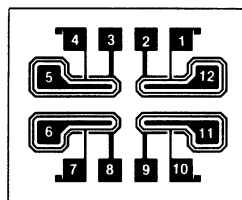
P_D Total Package Power Dissipation (at or below $T_A = +25^\circ\text{C}$)	640mW
Linear Derating Factor	10.7mW/ $^\circ\text{C}$
P_D Single Device Power Dissipation (at or below $T_A = +25^\circ\text{C}$)	300mW
Linear Derating Factor	5.0mW/ $^\circ\text{C}$
T_j Operating Junction Temperature Range	-55 to +85 $^\circ\text{C}$
T_S Storage Temperature Range	-55 to +150 $^\circ\text{C}$

SCHEMATIC DIAGRAM



Note: Pin numbers correspond to Package Pin-out

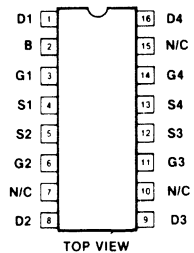
CHIP CONFIGURATION



PAD NO.	PAD FUNCTION	PAD NO.	PAD FUNCTION
1	Gate No. 1	7	Gate No. 3
2	Source No. 1	8	Source No. 3
3	Source No. 2	9	Source No. 4
4	Gate No. 2	10	Gate No. 4
5	Drain No. 2	11	Drain No. 4
6	Drain No. 3	12	Drain No. 1

Dimensions: .041 x .033 x .013 inches

PIN CONFIGURATION



DIMENSIONS
16-Pin Plastic DIP
See Package 10

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC		SD5200			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
1	STATIC	BV_{DS} Drain-Source Breakdown Voltage	30	35		V	$I_D = 10\mu\text{A}, V_{GS} = V_{BS} = 0$	
2		BV_{SB} Source-Substrate Breakdown Voltage	15			V	$I_S = 10\mu\text{A}, V_{GB} = 0$ Drain Open	
3		I_{GBS} Gate-Body Leakage Current			1.0	μA	$V_{GB} = 25\text{V}, V_{DB} = V_{SB} = 0$	
4		$V_{GS(th)}$ Gate-Source Threshold Voltage	0.5	1.0	2.0	V	$V_{DS} = V_{GS}, I_D = 1.0\mu\text{A}$ $V_{SB} = 0$	
5		$r_{DS(on)}$ Drain-Source ON Resistance		50	80	ohms	$V_{GS} = 5\text{V}$	$I_D = 1\text{mA}$ $V_{SB} = 0$
6				30		ohms	$V_{GS} = 10\text{V}$	
7				23		ohms	$V_{GS} = 15\text{V}$	
8				19		ohms	$V_{GS} = 20\text{V}$	
9	DYNAMIC	g_{fs} Common-Source Forward Transconductance	10	12		mmhos	$V_{DS} = 10\text{V}, I_D = 20\text{mA}$ $f = 1\text{KHz}, V_{SB} = 0$	
10		$C_{(gs + gd + gb)}$ Gate Node Capacitance		2.4	3.5	pF	$f = 1\text{MHz}$ $V_{DS} = 10\text{V}$ $V_{GS} = V_{BS} = -15\text{V}$	
11		$C_{(gd + db)}$ Drain Node Capacitance		1.3	1.5	pF		
12		$C_{(gs + sb)}$ Source Node Capacitance		3.5	4.0	pF		
13		$C_{(dg)}$ Reverse Transfer Capacitance		0.3	0.5	pF		
14		C_T Cross Talk		-107		dB		

QUAD D-MOS FET ANALOG SWITCH ARRAYS

ORDERING INFORMATION



FEATURES

- Low Interelectrode Capacitances
 Analog Input—3.5pF typ.
 Input (Gate) —2.4pF typ.
 Output —1.3pF typ.
 Feedback —0.3pF typ.
- Low Insertion Loss, $r_{DS} < 30$ ohms
- Low Crosstalk—-107dB @ 3KHz
- Bidirectional Switches
- Small-Outline Surface Mount Package

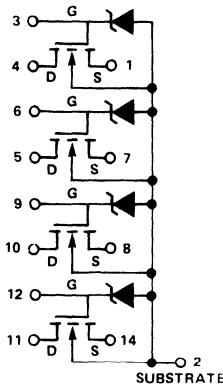
APPLICATIONS

- High Speed Analog Switches
 Analog Range $\pm 10V$ —SD5400
 Analog Range $\pm 7.5V$ —SD5402
 Analog Range $\pm 5.0V$ —SD5401
- High-Speed Switch Drivers
 20V—SD5400
 15V—SD5402
 10V—SD5401
- Sample & Hold

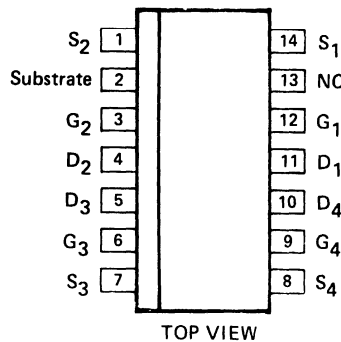
ABSOLUTE MAXIMUM RATINGS (T_c = +25°C unless otherwise noted)

PARAMETER	SD5400	SD5401	SD5402	UNITS	
V _{DS}	+20	+10	+15	V	I _D Continuous Drain Current 50mA
V _{SD}	+20	+10	+15	V	P _D Total Package Power Dissipation (at or below T _A = +25°C) 640mW
V _{DB}	+25	+15	+22.5	V	Linear Derating Factor 5.33mW/°C
V _{SB}	+25	+15	+22.5	V	P _D Single Device Power Dissipation (at or below T _A = +25°C) 300mW
V _{GS}	-25	-15	-22.5	V	T _J Operating Junction Temperature Range 0 to +70°C
	+30	+25	+30	V	T _S Storage Temperature Range -55 to +125°C
V _{GB}	-0.3	-0.3	-0.3	V	
	+30	+25	+30	V	
V _{GD}	-25	-15	-22.5	V	
	+30	+25	+30	V	

SCHEMATIC DIAGRAM



PIN CONFIGURATION



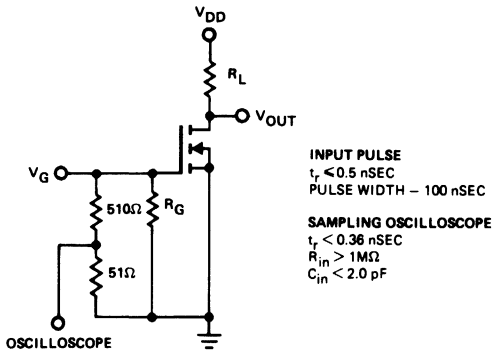
PACKAGE DIMENSIONS SO-14

(See Package 20)

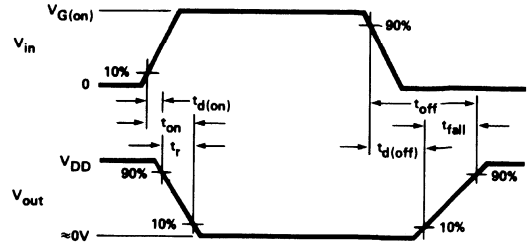
ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$, per channel, unless otherwise noted)

#	PARAMETER	SD5400			SD5401			SD5402			UNIT	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
1	BV_{DS} Drain-Source Breakdown Voltage	20	25		10	25		15	25		V	$I_D = 10\text{nA}$ $V_{GS} = V_{BS} = -5\text{V}$
2	BV_{SD} Source-Drain Breakdown Voltage	20			10			15			V	$I_S = 10\text{nA}$ $V_{GD} = V_{BD} = -5\text{V}$
3	BV_{DB} Drain-Substrate Breakdown Voltage	25			15			22.5			V	$I_D = 10\text{nA}$, $V_{GB} = 0$ Source Open
4	BV_{SB} Source-Substrate Breakdown Voltage	25			15			22.5			V	$I_S = 10\mu\text{A}$, $V_{GB} = 0$ Drain Open
5	$I_{D(off)}$ Drain-Source Off Current						10				nA	$V_{DS} = 10\text{V}$
6									10		nA	$V_{DS} = 15\text{V}$
7				10							nA	$V_{DS} = 20\text{V}$
8	$I_{S(off)}$ Source-Drain OFF Current						10				nA	$V_{SD} = 10\text{V}$
9									10		nA	$V_{SD} = 15\text{V}$
10				10							nA	$V_{SD} = 20\text{V}$
11	I_{GBS} Gate-Body Leakage Current						1.0				μA	$V_{GB} = 25\text{V}$
12				1.0						1.0	μA	$V_{GB} = 30\text{V}$
13	$V_{GS(th)}$ Gate Threshold Voltage	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1\mu\text{A}$ $V_{SB} = 0$
14	$r_{DS(on)}$ Drain-Source ON Resistance		50	70		50	70		50	70	ohms	$V_{GS} = 5\text{V}$
15			30			30			30			$V_{GS} = 10\text{V}$
16			23			23			23			$V_{GS} = 15\text{V}$
17			19			19			19			$V_{GS} = 20\text{V}$
18	r_{DSM} ON Resistance Match		1.0	5.0		1.0	5.0		1.0	5.0		$V_{GS} = 5\text{V}$
19	θ_{fs} Common-Source Forward Transcond.	10	12		10	12		10	12		mmhos	$V_{DS} = 10\text{V}$, $I_D = 20\text{mA}$ $f = 1\text{KHz}$, $V_{SB} = 0$
20	$C_{(gs + gd + gb)}$ Gate Node Capacitance		2.4	3.5		2.4	3.5		2.4	3.5	pF	$V_{DS} = 10\text{V}$ $V_{GS} = V_{BS} = -15\text{V}$ $f = 1\text{MHz}$
21	$C_{(gs + db)}$ Drain Node Capacitance		1.3	1.5		1.3	1.5		1.3	1.5		
22	$C_{(gs + sb)}$ Source Node Capacitance		3.5	4.0		3.5	4.0		3.5	4.0		
23	$C_{(dg)}$ Reverse Transfer Capacitance		0.3	0.5		0.3	0.5		0.3	0.5		
24	C_T Cross Talk		-107			-107			-107		dB	$f = 3\text{KHz}$, $R_G = 800\Omega$
25	$t_{d(on)}$ Turn ON Delay Time		0.7	1.0		0.7	1.0		0.7	1.0	nSec	$V_{DD} = 5\text{V}$, $V_{G(on)} = 10\text{V}$ $R_L = 680\Omega$, $R_G = 51\Omega$
26	t_r Rise Time		0.8	1.0		0.8	1.0		0.8	1.0		
27	t_{off} Turn OFF Time		10			10			10			

SWITCHING TIMES TEST CIRCUIT

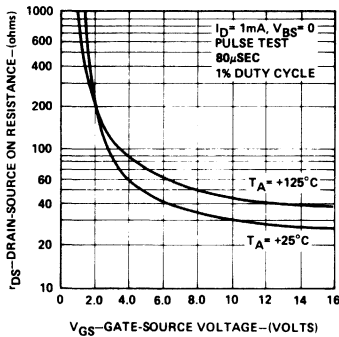


TEST WAVEFORMS

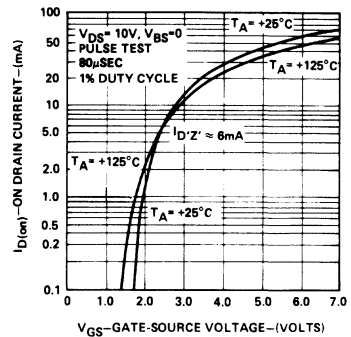


TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$, per channel, unless otherwise specified)

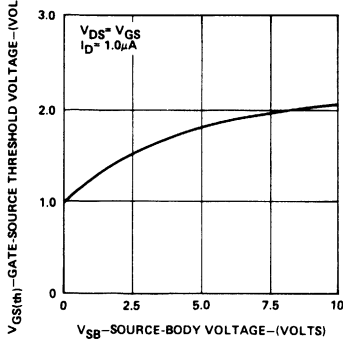
DRAIN-SOURCE ON RESISTANCE
—vs—
GATE-SOURCE VOLTAGE



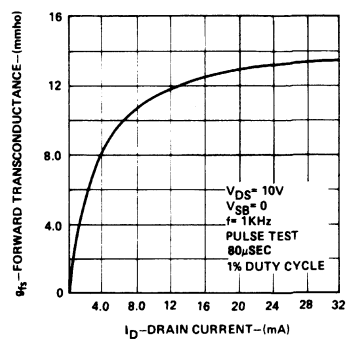
ON DRAIN CURRENT
—vs—
GATE-SOURCE VOLTAGE



GATE-SOURCE THRESHOLD VOLTAGE
—vs—
SOURCE-BODY VOLTAGE



FORWARD TRANSCONDUCTANCE
—vs—
ON DRAIN CURRENT



N-CHANNEL DEPLETION-MODE 4-CHANNEL D-MOS FET ARRAY

ORDERING INFORMATION



FEATURES

- Normally ON Configuration
- Low Interelectrode Capacitances
- High-Speed Switching
- Wide Dynamic Range

APPLICATIONS

- High-Speed Analog Switches
- Wide-Band Dual Differential Amplifiers
- Dual Cascode Amplifiers
- High Intercept Point Double Balanced Mixers

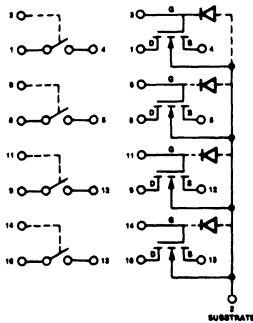
ABSOLUTE MAXIMUM RATINGS (per channel,

$T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DS} Drain-Source Voltage	+30Vdc
V_{SD} Source-Drain Voltage	+0.5Vdc
V_{DB} Drain-Body Voltage	+30Vdc
V_{SB} Source-Body Voltage	+15Vdc
V_{GS} Gate-Source Voltage	+25Vdc
V_{GB} Gate-Body Voltage	+25Vdc
Gate-Body Voltage	-0.3Vdc
V_{GD} Gate-Drain Voltage	+25Vdc
I_D Continuous Drain Current	50mA

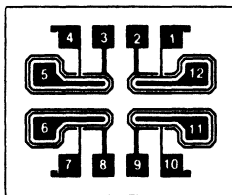
P_D Total Package Power Dissipation (at or below $T_A = +25^\circ\text{C}$)	640mW
Linear Derating Factor	10.7mW/ $^\circ\text{C}$
P_D Single Device Power Dissipation (at or below $T_A = +25^\circ\text{C}$)	300mW
Linear Derating Factor	5.0mW/ $^\circ\text{C}$
T_j Operating Junction Temperature Range	-55 to +85 $^\circ\text{C}$
T_S Storage Temperature Range	..	-55 to +150 $^\circ\text{C}$

SCHEMATIC DIAGRAM



Note: Pin numbers correspond to Package Pin-out

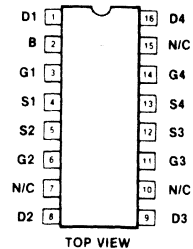
CHIP CONFIGURATION



PAD NO.	PAD FUNCTION	PAD NO.	PAD FUNCTION
1	Gate No. 1	7	Gate No. 3
2	Source No. 1	8	Source No. 3
3	Source No. 2	9	Source No. 4
4	Gate No. 2	10	Gate No. 4
5	Drain No. 2	11	Drain No. 4
6	Drain No. 3	12	Drain No. 1

Dimensions: .041 × .033 × .013 Inches

PIN CONFIGURATION



DIMENSIONS

16-Pin Plastic DIP
See Package 10

16-Pin Ceramic DIP
See Package 15

ELECTRICAL CHARACTERISTICS (per channel, $T_A = +25^\circ\text{C}$, unless otherwise noted)

#	CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS		
1	STATIC	BV_{DS} Drain-Source Breakdown Voltage	20			V	$I_D = 10\text{ nA}, V_{GS} = V_{BS} = -5\text{V}$		
2		BV_{SD} Source-Drain Breakdown Voltage	10				$I_S = 10\text{ nA}, V_{GD} = V_{BD} = -5\text{V}$		
3		BV_{DB} Drain-Body Breakdown Voltage	25				$I_D = 10\text{ nA}, V_{GB} = 0$ Source Open		
4		BV_{SB} Source-Body Breakdown Voltage	15				$I_S = 10\text{ }\mu\text{A}, V_{GB} = 0$ Drain open		
5		$I_{GSS(fwd)}$ Forward Gate Leakage Current			1.0	nA	$V_{GS} = 25\text{V}, V_{DS} = V_{BS} = 0$		
6		I_G Gate Operating Current			-3.0	-100	pA	$V_{DG} = 20\text{V}$ $I_D = 5.0\text{ mA}$	$T_A = +125^\circ\text{C}$
7					-0.7	-10	nA	$V_{BS} = -5.6\text{V}$	
8		$V_{GS(off)}$ Gate-Source Cutoff Voltage	-1.0		-5.0	V	$V_{DS} = 10\text{V}, I_D = 1.0\text{ }\mu\text{A}$ $V_{BS} = -5.6\text{V}$		
9		$V_{GS(on)}$ Gate-Source ON Voltage	-0.3		-3.0		$V_{DG} = 10\text{V}, I_D = 5\text{ mA}, V_{SB} = -5.6\text{V}$		
10		I_{DSX} Zero Gate Voltage ⁽¹⁾ Drain Current		7.0		40	mA	$V_{DS} = 10\text{V}$ $V_{GS} = 0$	$T_A = +125^\circ\text{C}$
11				5.0				$V_{BS} = -5.6\text{V}$	
12		$r_{DS(ON)}$ Drain-Source ON Resistance		100	150	ohms	$I_D = 1.0\text{ mA}, V_{GS} = 0, V_{BS} = -5.6\text{V}$		
13	DYNAMIC	g_{fs} Common-Source ⁽¹⁾ Forward Transconductance	5.0	7.5	10	mmhos	$V_{DG} = 10\text{V}$ $I_D = 5.0\text{ mA}$ $V_{BS} = -5.6\text{V}$	f = 1 KHz	
14		g_{os} Common-Source Output Conductance		200	300	μmhos			
15		C_{iss} Common-Source Input Capacitance		3.5		pF		f = 1 MHz	
16		C_{oss} Common-Source Output Capacitance		1.2					
17		C_{rss} Common-Source Reverse Transfer Capacitance		0.3					
18		$C_{(gs + sb)}$ Source Node Capacitance		4.5					
19	MATCHING	V_{GSM} Gate Source ⁽²⁾ Voltage Match		50		mV			
20		$r_{DS(on)}$ Drain-Source ^{(1), (2)} ON Resistance Match	0.90	0.98	1.0		$I_D = 1.0\text{ mA}, V_{GS} = 0, V_{BS} = 5.6\text{V}$		
21		I_{DSXM} Zero Gate Voltage ^{(1), (2)} Drain Current Match	0.90		1.0		$V_{DG} = 10\text{V}$ $I_D = 5.0\text{ mA}$	f = 1 KHz	
22		g_{fsm} Transconductance Match ^{(1), (2)}	0.90		1.0		$V_{BS} = -5.6\text{V}$		

Note 1: Pulse Test, 80 μsec , 1% Duty Cycle

Note 2: Match of 4 channels

TYPICAL PERFORMANCE CHARACTERISTICS: SEE TZ5911

N-CHANNEL ENHANCEMENT-MODE D-MOS FET SWITCHES

ORDERING INFORMATION

Part Number	Package	Temp. Range	Lead Type
SST211	SOT-143	-55 to +125°C	Gold Wire
SST213	SOT-143	-55 to +125°C	Gold Wire
SST215	SOT-143	-55 to +125°C	Gold Wire

FEATURES

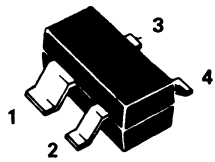
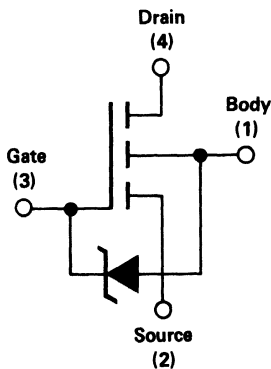
- Low Transfer Capacitance, c_{rss} 0.3 pF typ.
- High Speed Switching, t_{on} <2nSec.
- Surface Mount Package

APPLICATIONS

- +30V Switch Driver - SST 211
- ±10V Analog Switch - SST 21
- ±5V Analog Switch - SST 213
- Sample & Hold
- Multiplexers

ABSOLUTE MAXIMUM RATINGS ($T_c = +25^\circ\text{C}$ unless otherwise noted)

PARAMETER BREAKDOWN VOLTAGES	SST 211	SST 213	SST 215	UNIT	
V_{DS}	+30	+10	+20	Vdc	I_D Continuous Drain Current 50 mA
V_{SD}	+10	+10	+20	Vdc	P_T Power Dissipation (at or below $T_c = +25^\circ\text{C}$) 360 mW
V_{DB}	+30	+15	+25	Vdc	Linear Derating Factor 3.6 mW/°
V_{SB}	+15	+15	+25	Vdc	T_J Operating Junction Temperature Range -55 to +125°C
V_{GS}	-15	-15	-25	Vdc	T_s Storage Temperature Range . . -55 to +150°C
V_{GB}	+25	+25	+30	Vdc	
V_{GB}	-0.3	-0.3	-0.3	Vdc	
V_{GD}	+25	+25	+30	Vdc	
V_{GD}	-30	-15	-25	Vdc	
V_{GD}	+25	+25	+30	Vdc	



PACKAGE DIMENSIONS SOT-143

See Package 24

ELECTRICAL CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise noted)

#	PARAMETER		SST211			SST213			SST215			UNIT	TEST CONDITIONS	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	BV _{DS}	Drain-Source Breakdown Voltage	30	35								V	I _D = 10μA V _{GS} = V _{BS} = 0	
2			10	25		10	25		20	25			I _D = 10nA V _{GS} = V _{BS} = -5V	
3	BV _{SD}	Source-Drain Breakdown Voltage	10		10			20	22		I _S = 10nA V _{GD} = V _{BD} = -5V			
4	BV _{DB}	Drain-Substrate Breakdown Voltage	15		15			25	40		I _D = 10nA, V _{GB} = 0 Source OPEN			
5	BV _{SB}	Source-Substrate Breakdown Voltage	15		15			25	40		I _S = 10μA, V _{GB} = 0 Drain OPEN			
6	I _{D(off)}	Drain-Source OFF Current		0.2	10		0.2	10				nA	V _{DS} = 10V V _{GS} = V _{BS} = -5V	
7		Source-Drain OFF Current		0.6	10		0.6	10			0.2		10	V _{SD} = 10V V _{GD} = V _{BD} = -5V
8	I _{S(off)}	Source-Drain OFF Current		0.6	10		0.6	10			0.6		10	V _{SD} = 20V V _{DB} = V _{SB} = 0
9	I _{GBS}	Gate-Body Leakage Current			10			10					10	V _{GB} = 25V V _{DS} = V _{GS}
10	V _{GS(th)}	Gate Threshold Voltage	0.5	1.0	2.0	0.1		2.0	0.1	1.0	2.0	V	I _D = 1μA, V _{SB} = 0	
11														10
12	r _{DS(on)}	Drain-Source ON Resistance (1)		50	70		50	70		50	70	ohms	V _{GS} = 5V I _D = 1mA	
13	r _{DS(on)}	Drain-Source ON Resistance		30	45		30	45		30	45		V _{GS} = 10V V _{SB} = 0	
14	g _{fs}	Common-Source (1) Forward Transcond.	10	12		10	12		10	12		mmhos	V _{DS} = 10V, I _D = 20mA f = 1KHz, V _{SB} = 0	
15	C _(gs-gd-gb)	Gate Node Capacitance		2.4	3.5		2.4	3.5		2.4	3.5		pF	V _{DS} = 10V V _{GS} = V _{BS} = -15V f = 1MHz
16	C _(gd-db)	Drain Node Capacitance		1.3	1.5		1.3	1.5		1.3	1.5			
17	C _(gs-ab)	Source Node Capacitance		3.5	4.0		3.5	4.0		3.5	4.0			
18	C _(dg)	Reverse Transfer Capacitance		0.3	0.5		0.3	0.5		0.3	0.5			
19	t _{d(on)}	Turn ON Delay Time		0.7	1.0		0.7	1.0		0.7	1.0	nSec		V _{DD} = 5V, V _{G(on)} = 10V R _L = 680Ω, R _G = 51Ω
20	t _r	Rise Time		0.8	1.0		0.8	1.0		0.8	1.0			
21	t _{off}	Turn OFF Time		10			10			10				
22														

Note 1: Pulse Test, 80μ Sec, 1% Duty Cycle
Typical Performance Characteristics: See SD210-215 Series

N-CHANNEL ENHANCEMENT-MODE D-MOS FETs

ORDERING INFORMATION



FEATURES

- Reliable, low cost, plastic package
- High Speed Switching, $t_r < 1\text{nSec}$
- Low Capacitance, c_{rss} 0.3 pF typ
- CMOS and TTL Compatible Input

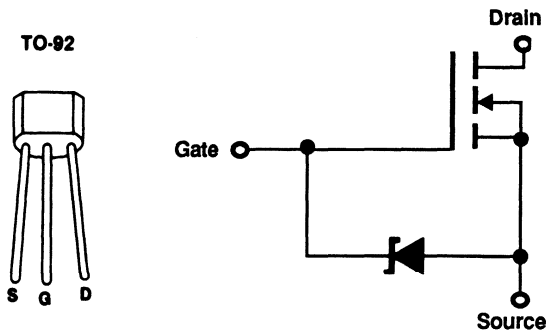
APPLICATIONS

- Switch Drivers
- Video Switches
- Active Pullups
- VHF/UHF Amplifiers

ABSOLUTE MAXIMUM RATINGS ($T_C = +25^\circ\text{C}$ unless otherwise noted)

Drain-Source Voltage		Source-Drain Voltage	-0.3V
TZ400	+30V	Continuous Drain Current	50mA
TZ402	+15V	Power Dissipation (at or below	
Gate-Source Voltage	-0.3V	$T_C = +25^\circ\text{C}$)	300mW
	+20V	Linear Derating Factor	3.0mW/°C
Gate-Drain Voltage	-0.3V	Operating Storage and	
	+20V	Junction Temperature Range	-40°C to +125°C

PIN CONFIGURATION/SCHEMATIC DIAGRAM



PACKAGE DIMENSIONS (TO-92) TO-226AA

See Package 5

ELECTRICAL CHARACTERISTICS ($T_C = +25^\circ\text{C}$)

#	CHARACTERISTIC	TZ400			TZ402			UNIT	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
1	BV_{DS} Drain-Source Breakdown Voltage	30	35		15	25		V	$I_D = 1.0\mu\text{A}, V_{GS} = 0$
2	$I_{D(off)}$ Drain-Source OFF Leakage Current			1.0			1.0	μA	$V_{DS} = 15\text{V}, V_{GS} = 0$
3	I_{GSS} Gate-Source Leakage Current			1.0			1.0	μA	$V_{GS} = 20\text{V}, V_{DS} = 0$
4	$I_{D(on)}$ Drain-Source ON Current	50	100		50	100		mA	$V_{DS} = 10\text{V}, V_{GS} = 10\text{V}$ Pulse Test
5	$V_{GS(th)}$ Gate-Source Threshold Voltage	0.7		1.5	0.7		1.5	V	$I_D = 1.0\mu\text{A}, V_{DS} = V_{GS}$
6	$V_{DS(on)}$ Drain-Source ON Voltage		150	250		150	250	mV	$I_D = 1\text{mA}, V_{GS} = 2.4\text{V}$
7	$r_{DS(on)}$ Drain-Source ON Resistance		150	250		150	250	ohms	
8	$V_{DS(on)}$ Drain-Source ON Voltage		60	80		60	80	mV	$I_D = 1\text{mA}, V_{GS} = 4.5\text{V}$
9	$r_{DS(on)}$ Drain-Source ON Resistance		60	80		60	80	ohms	
10	g_{fs} Common-Source Forward Transcond.	8.0	12		8.0	12		mmhos	$I_D = 20\text{mA}, V_{DS} = 10\text{V}$ $f = 1\text{KHz}$ Pulse Test
11	C_{iss} Common-Source Input Capacitance		4.0	5.0		4.0	5.0	pf	$V_{DS} = 10\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$
12	C_{oss} Common-Source Output Capacitance		1.8	2.5		1.8	2.5		
13	C_{rss} Common-Source Reverse Transfer Capacitance		0.3	0.5		0.3	0.5		
14	$t_{d(on)}$ Turn ON Delay Time		0.7	1.0		0.7	1.0	nS	$V_{DD} = 10\text{V}, R_L = 680\Omega$ $V_{GS(on)} = 10\text{V}, R_G = 51\Omega$ $C_L = 1.5\text{pF}$
15	t_r Rise Time		0.8	1.0		0.8	1.0		
16	$t_{f(off)}$ Turn OFF Time		12			12			

SWITCHING TIMES TEST CIRCUIT

Input Pulse

$t_r \leq 0.5nSEC$

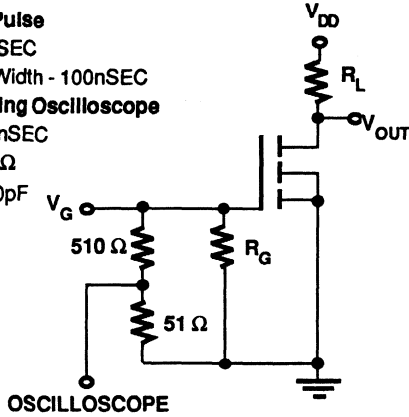
Pulse Width - 100nSEC

Sampling Oscilloscope

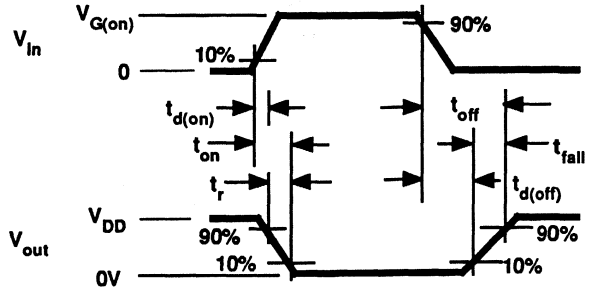
$t_r < 0.36nSEC$

$R_{in} > 1M\Omega$

$C_{in} < 2.0pF$

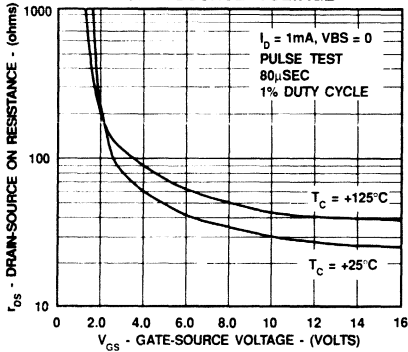


TEST WAVEFORMS

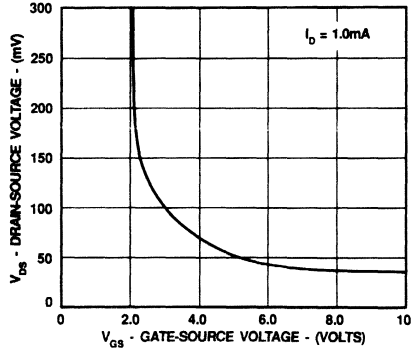


TYPICAL PERFORMANCE CHARACTERISTICS ($T_C = +25^\circ C$ unless otherwise noted)

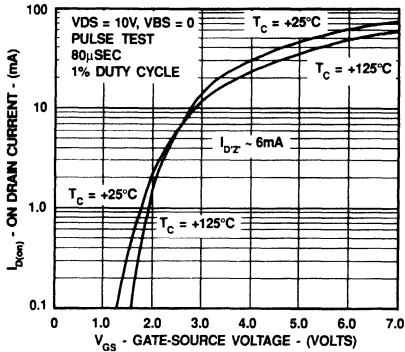
DRAIN-SOURCE ON RESISTANCE
-vs-
GATE-SOURCE VOLTAGE



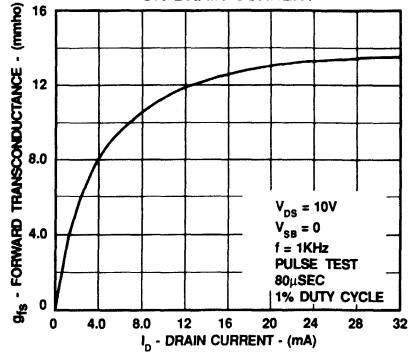
DRAIN-SOURCE ON VOLTAGE
-vs-
GATE-SOURCE VOLTAGE



ON DRAIN CURRENT
-vs-
GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE
-vs-
ON DRAIN CURRENT



N-CHANNEL ENHANCEMENT-MODE D-MOS FET ULTRA HIGH-SPEED LOW-COST SWITCH

ORDERING INFORMATION

TO-92 Plastic Package	TZ4O3BD
Description	15V, 60 ohm

FEATURES

- Reliable, Low Cost, Plastic Package
- High Speed Switching, $t_r < 1\text{nSec}$
- Low Capacitance, c_{rss} 0.4pF typ
- CMOS and TTL Compatible Input

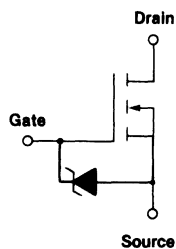
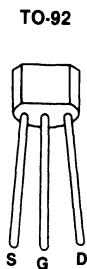
APPLICATIONS

- Switch Drivers
- Video Switches
- Sample Hold and Track and Hold
- VHF/UHF Amplifiers

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

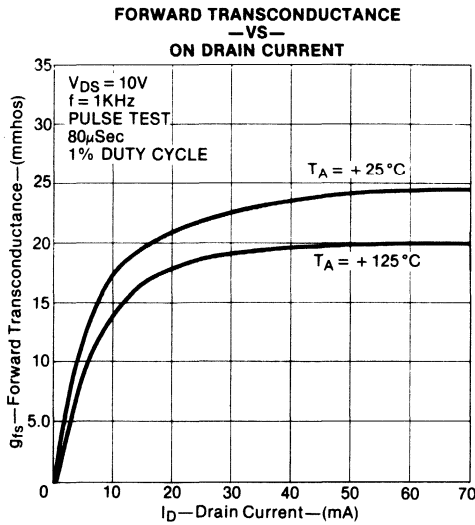
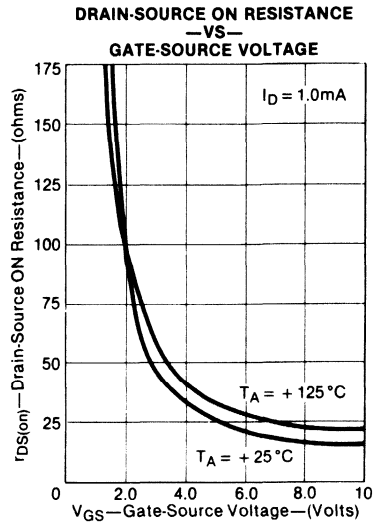
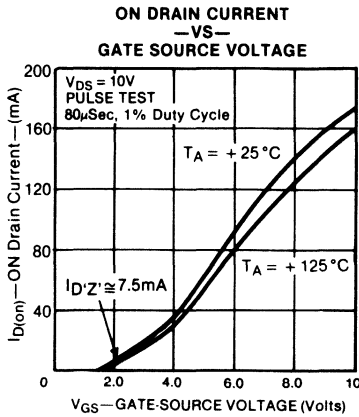
Drain-Source Voltage	+15V	Continuous Drain Current	50mA
Gate-Source Voltage	-0.3V	Power Dissipation (at or below $T_A = +25^\circ\text{C}$)	300mW
	+20V	Linear Derating Factor	3.0mW/ $^\circ\text{C}$
Gate-Drain Voltage	-0.3V	Operating Storage and	
	+20V	Junction Temperature Range	-40 $^\circ\text{C}$ to +125 $^\circ\text{C}$
Source-Drain Voltage	-0.3V		

PIN CONFIGURATION/SCHEMATIC DIAGRAM



PACKAGE DIMENSIONS (TO-92) TO-226AA (See Package 5)

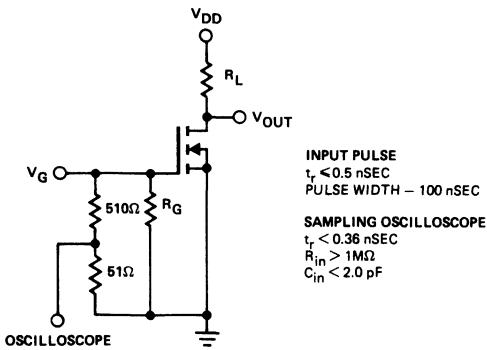
TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)



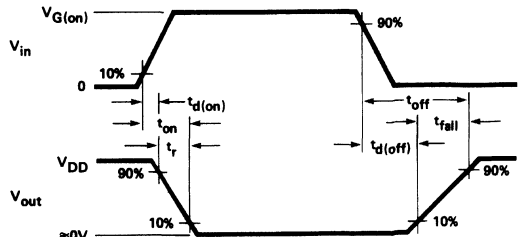
ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITION
STATIC	BV_{DS} Drain-Source Breakdown Voltage	15	25		V	$I_D = 1.0\mu\text{A}$, $V_{GS} = 0$
	$I_{D(off)}$ Drain-Source OFF Leakage Current			1.0	μA	$V_{DS} = 15\text{V}$, $V_{GS} = 0$
	I_{GSS} Gate-Source Leakage Current			1.0	μA	$V_{GS} = 20\text{V}$, $V_{DS} = 0$
	$I_{D(on)}$ Drain-Source ON Current	80	120		mA	$V_{DS} = 10\text{V}$, $V_{GS} = 10\text{V}$ Pulse Test
	$V_{GS(th)}$ Gate-Source Threshold Voltage	0.7		1.5	V	$I_D = 1.0\mu\text{A}$, $V_{DS} = V_{GS}$
	$V_{DS(on)}$ Drain-Source ON Voltage		140	175	mV	$I_D = 1\text{mA}$, $V_{GS} = 2.4\text{V}$
	$r_{DS(on)}$ Drain-Source ON Resistance		140	175	ohms	
	$V_{DS(on)}$ Drain-Source ON Voltage		40	60	mV	$I_D = 1\text{mA}$, $V_{GS} = 4.5\text{V}$
	$r_{DS(on)}$ Drain-Source ON Resistance		40	60	ohms	
DYNAMIC	g_{fs} Common-Source Forward Transcond.	15	19		mmhos	$I_D = 20\text{mA}$, $V_{DS} = 10\text{V}$ $f = 1\text{KHz}$ Pulse Test
	C_{iss} Common-Source Input Capacitance		4.5	6.0	pf	$V_{DS} = 10\text{V}$, $V_{GS} = 0$ $f = 1\text{MHz}$
	C_{oss} Common-Source Output Capacitance		2.0	3.0		
	C_{rss} Common-Source Reverse Transfer Capacitance		0.4	0.6		
	$t_{d(on)}$ Turn ON Delay Time		0.8	1.2	nS	$V_{DD} = 10\text{V}$, $R_L = 680\Omega$ $V_{G(on)} = 10\text{V}$, $R_G = 51\Omega$ $C_L = 1.5\text{pF}$
	t_r Rise Time		0.9	1.2		
t_{off} Turn OFF Time		14				

SWITCHING TIMES TEST CIRCUIT



TEST WAVEFORMS



N-CHANNEL ENHANCEMENT-MODE D-MOS FET ULTRA HIGH-SPEED LOW-COST SWITCH

ORDERING INFORMATION



FEATURES

- Reliable, Low Cost, Plastic Package
- High Speed Switching, $t_r < 2\text{nSec}$
- Low Capacitance, c_{rss} 1.2 pF typ
- CMOS and TTL Compatible Input
- Available in Surface Mount Package

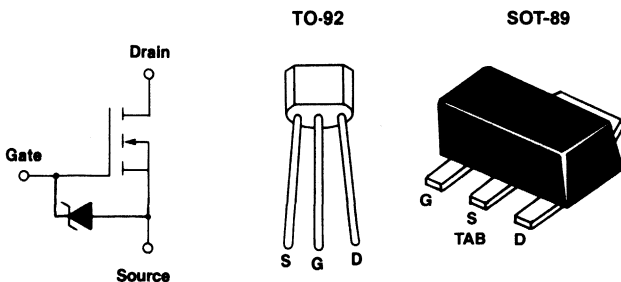
APPLICATIONS

- Switch Drivers
- Video Switches
- VHF/UHF Amplifiers

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

Drain-Source Voltage	+20V	Peak Pulsed Drain Current	+0.8A
Gate-Source Voltage	-0.3V	Continuous Drain Current	100mA
	+20V	Power Dissipation (at or below $T_A = +25^\circ\text{C}$)	300mW
Gate-Drain Voltage	-0.3V	Linear Derating Factor	3.0mW/ $^\circ\text{C}$
	+20V	Operating Junction and	
Source-Drain Voltage	-0.3V	Storage Temperature Range	-40 $^\circ\text{C}$ to +125 $^\circ\text{C}$

PIN CONFIGURATIONS



PACKAGE DIMENSIONS

TO-92

TO-226AA (TO-92)
See Package 5

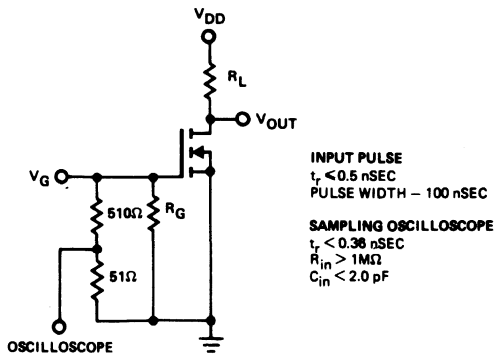
TO-243AA (SOT-89)
See Package 23

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

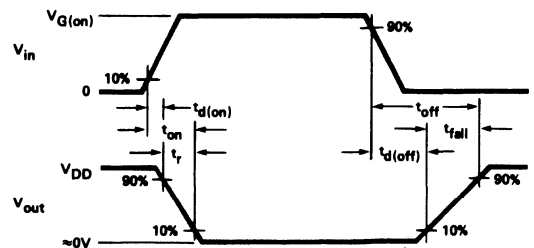
CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITION
STATIC	BV_{DS} Drain-Source Breakdown Voltage	20	25		V	$I_D = 1.0\mu\text{A}$, $V_{GS} = 0$
	$I_{D(off)}$ Drain-Source OFF Leakage Current			1.0	μA	$V_{DS} = 15\text{V}$, $V_{GS} = 0$
	I_{GSS} Gate-Source Leakage Current			10	μA	$V_{GS} = 20\text{V}$, $V_{DS} = 0$
	$I_{D(on)}$ Drain-Source ON Current	0.8	1.2		A	$V_{DS} = 10\text{V}$, $V_{GS} = 10\text{V}$ (Note 1)
	$V_{GS(th)}$ Gate-Source Threshold Voltage	0.7	1.1	1.5	V	$I_D = 1.0\mu\text{A}$, $V_{DS} = V_{GS}$
	$V_{DS(on)}$ Drain-Source ON Voltage			200	mV	(Note 1)
	$r_{DS(on)}$ Drain-Source ON Resistance			20	ohms	
	$V_{DS(on)}$ Drain-Source ON Voltage			800	mV	
	$r_{DS(on)}$ Drain-Source ON Resistance			8.0	ohms	$I_D = 100\text{mA}$ $V_{GS} = 4.5\text{V}$
DYNAMIC	g_{fs} Common-Source Forward Transcond.	100			mmhos	$I_D = 0.3\text{A}$ $V_{DS} = 20\text{V}$ $f = 1\text{KHz}$
	C_{iss} Common-Source Input Capacitance		12	18	pf	$V_{DS} = 20\text{V}$, $V_{GS} = 0$ $f = 1\text{MHz}$
	C_{oss} Common-Source Output Capacitance		6.0	8.0		
	C_{rss} Common-Source Reverse Transfer Capacitance		1.2	2.0		
	$t_{d(on)}$ Turn ON Delay Time		1.0	1.5	nS	$V_{DD} = 10\text{V}$, $R_L = 390\Omega$ $V_{G(on)} = 10\text{V}$, $R_G = 51\Omega$ $C_L = 1.5\text{pF}$
	t_r Rise Time		1.0	2.0		
	$t_{(off)}$ Turn OFF Time		1.0			

Note 1: Pulse Test, 80 μSec , 1% Duty Cycle

SWITCHING TIMES TEST CIRCUIT

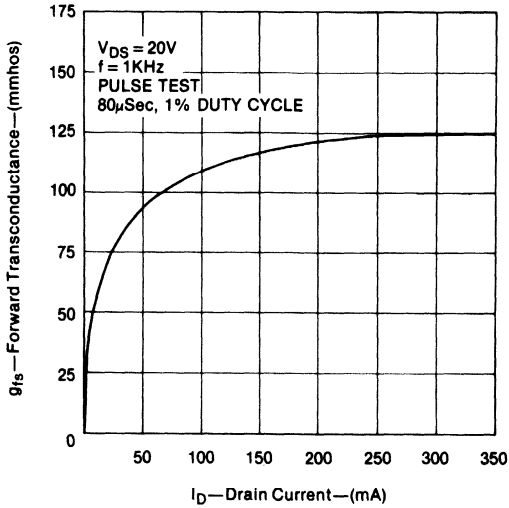


TEST WAVEFORMS

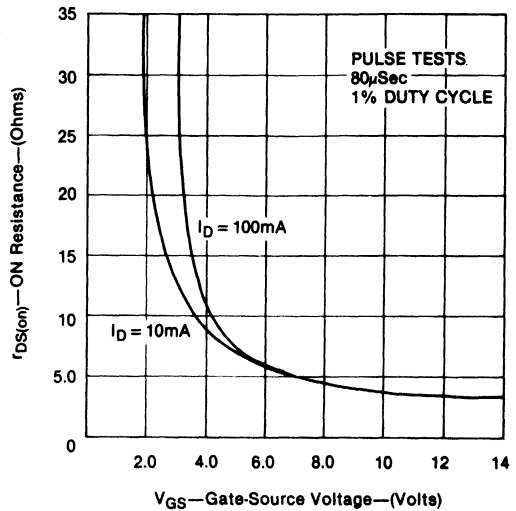


TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

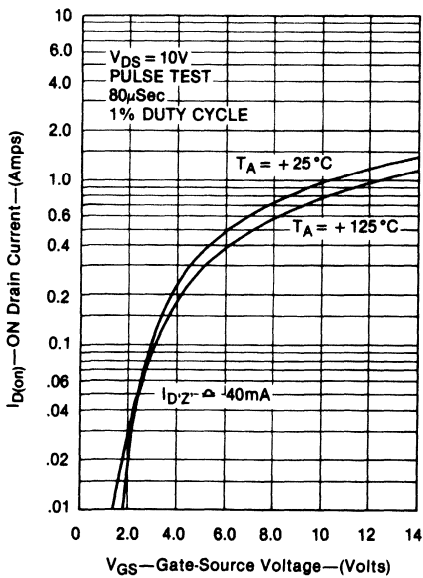
FORWARD TRANSCONDUCTANCE
—VS—
ON DRAIN CURRENT



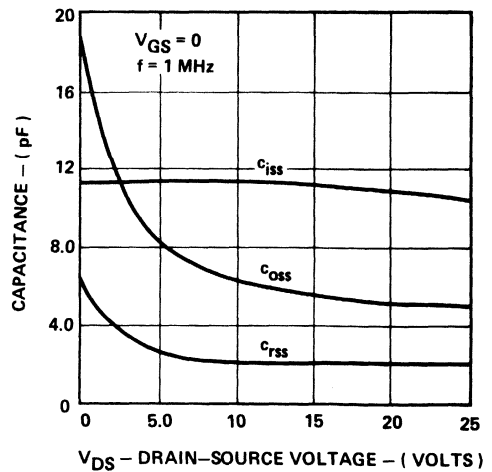
DRAIN-SOURCE ON RESISTANCE
—VS—
GATE-SOURCE VOLTAGE



ON DRAIN CURRENT
—VS—
GATE-SOURCE VOLTAGE



CAPACITANCES
—VS—
DRAIN-SOURCE VOLTAGE



N-CHANNEL DEPLETION-MODE DUAL D-MOS FET

ORDERING INFORMATION



FEATURES

- Normally ON Configuration
- Low Interelectrode Capacitances
- Available in surface mount package
- Pin and Function Compatible to Industry Standard Dual J-FETs with addition of Substrate Bias Pin

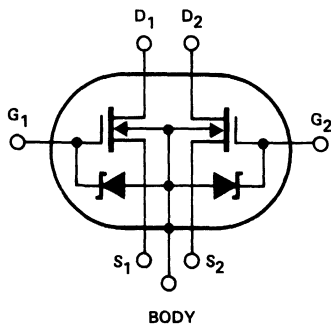
APPLICATIONS

- High-Speed Analog Comparators
- Wide-Band Differential Amplifiers
- Cascode Amplifiers
- High Intercept Point Balanced Mixers

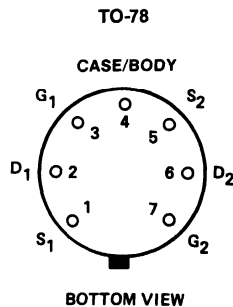
ABSOLUTE MAXIMUM RATINGS (per side, $T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DS} Drain-Source Voltage	+20V	I_D Continuous Drain Current	+50 mA
V_{SD} Source-Drain Voltage	+10V	P_D Device Dissipation (each side)	360 mW
V_{DB} Drain-Body Voltage	+25V	Derating Factor	2.88 mW/ $^\circ\text{C}$
V_{SB} Source-Body Voltage	+15V	P_D Total Device Dissipation	500 mW
V_{GD} Gate-Drain Voltage	+25V	Derating Factor	4 mW/ $^\circ\text{C}$
V_{GS} Gate-Source Voltage	+25V	Operating Junction and Storage	
V_{GB} Gate-Body Voltage	+25V	Temperature Range	-55 to +150 $^\circ\text{C}$
V_{G1G2} Gate-to-Gate Voltage	+25V	T_L Lead Temperature (1/16" from mounting	
V_{D1D2} Drain-to-Drain Voltage	+25V	surface for 10 sec.)	+260 $^\circ\text{C}$
V_{S1S2} Source-to-Source Voltage	+15V		

SCHEMATIC DIAGRAM

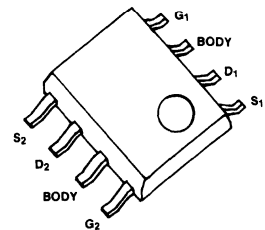


PIN CONFIGURATIONS



(See Package 4)

SO-8



(See Package 19)

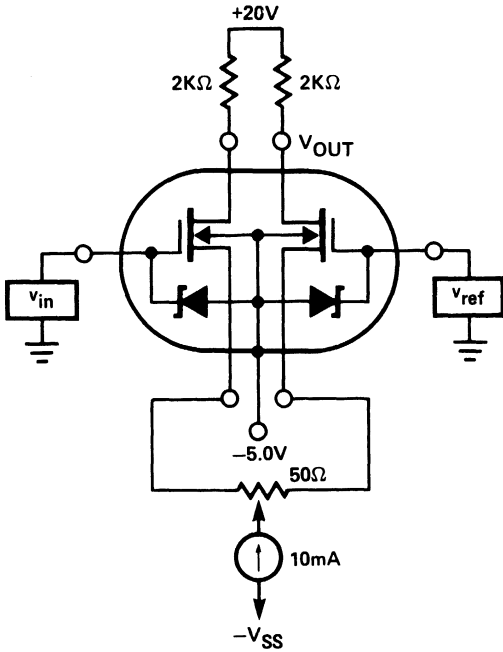
ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$, per side, unless otherwise noted)

#	CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
1	STATIC	BV_{DS} Drain-Source Breakdown Voltage	20			V	$I_D = 10\text{ nA}$, $V_{GS} = V_{BS} = -5\text{V}$	
2		BV_{SD} Source-Drain Breakdown Voltage	10				$I_S = 10\text{ nA}$, $V_{GD} = V_{BD} = -5\text{V}$	
3		BV_{DB} Drain-Body Breakdown Voltage	25				$I_D = 10\text{ nA}$, $V_{BB} = 0$ Source Open	
4		BV_{SB} Source-Body Breakdown Voltage	15				$I_S = 10\text{ }\mu\text{A}$, $V_{BB} = 0$ Drain open	
5		$I_{GSS}(fwd)$ Forward Gate Leakage Current			1.0	nA	$V_{GS} = 25\text{V}$, $V_{DS} = V_{BS} = 0$	
6		I_G Gate Operating Current		-3.0	-100	pA	$V_{DG} = 20\text{V}$ $I_D = 5.0\text{ mA}$ $V_{BS} = -5.6\text{V}$	
7				-0.7	-10	nA		$T_A = +125^\circ\text{C}$
8		$V_{GS(off)}$ Gate-Source Cutoff Voltage	-1.0		-5.0	V	$V_{DS} = 10\text{V}$, $I_D = 1.0\text{ nA}$ $V_{BS} = -5.6\text{V}$	
9		$V_{GS(on)}$ Gate-Source ON Voltage	-0.3		-3.0		$V_{DG} = 10\text{V}$, $I_D = 5\text{ mA}$, $V_{BS} = -5.6\text{V}$	
10		I_{DSX} Zero Gate Voltage ⁽¹⁾ Drain Current		7.0		mA	$V_{DS} = 10\text{V}$ $V_{GS} = 0$ $V_{BS} = -5.6\text{V}$	
11				5.0				$T_A = +125^\circ\text{C}$
12		$r_{DS(ON)}$ Drain-Source ON Resistance		100	150	ohms	$I_D = 1.0\text{ mA}$, $V_{GS} = 0$, $V_{BS} = -5.6\text{V}$	
13	DYNAMIC	g_{fs} Common-Source ⁽¹⁾ Forward Transcond.	5.0	7.5	10	mmhos	$V_{DG} = 10\text{V}$ $I_D = 5.0\text{ mA}$ $V_{BS} = -5.6\text{V}$	f = 1 KHz
14		g_{os} Common-Source Output Conductance		200		μmhos		f = 1 MHz
15		C_{iss} Common-Source Input Capacitance		3.5		pF		
16		C_{oss} Common-Source Output Capacitance		1.2				
17		C_{rss} Common Source Reverse Transfer Capacitance		0.3				
18	$C_{(gs + sb)}$ Source Node Capacitance		4.5					
19	MATCHING	$ V_{GS1} - V_{GS2} $ Differential Gate Source Voltage		20		mV	$V_{DG} = 10\text{V}$ $I_D = 5.0\text{ mA}$ $V_{BS} = -5.6\text{V}$	
20		$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$ Differential Drift		20		$\mu\text{V}/^\circ\text{C}$		$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$
21		$I_{DSX\ 1/2}$ Zero Gate Voltage ^{(1),(2)} Drain Current Ratio	0.90		1.0			
22		$g_{fs\ 1/2}$ Transcond. Ratio ^{(1),(2)}	0.90		1.0		f = 1 KHz	

Note 1: Pulse Test, 80 μsec , 1% Duty Cycle

Note 2: The lower value is side 1.

DIFFERENTIAL AMPLIFIER/COMPARATOR



PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$)

Low Frequency Differential Voltage Gain—6.2 min., 11.8 typ.

V_{in}, V_{ref} range—-5.0V to +10V

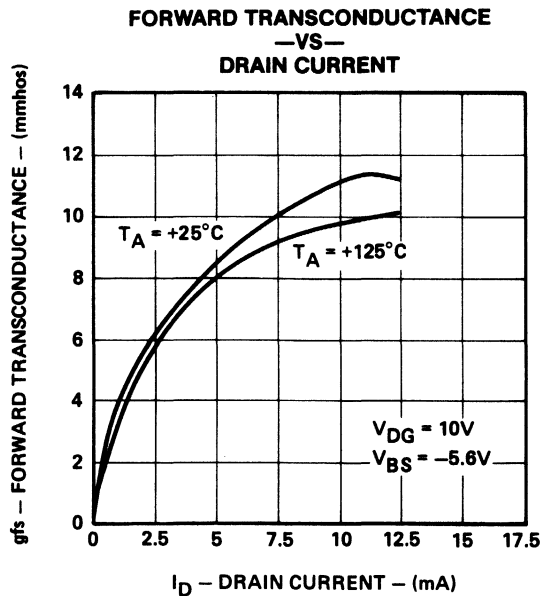
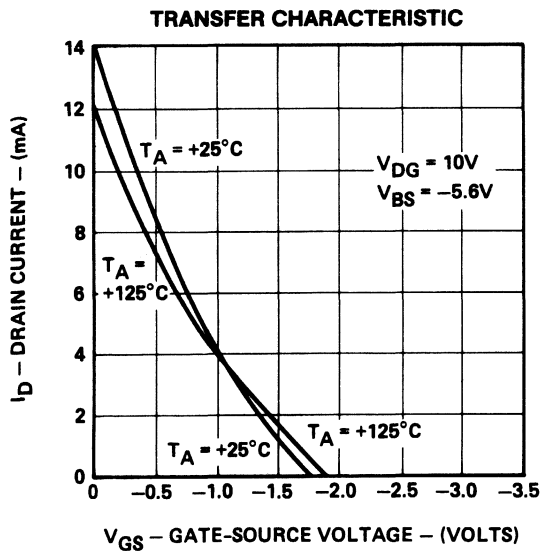
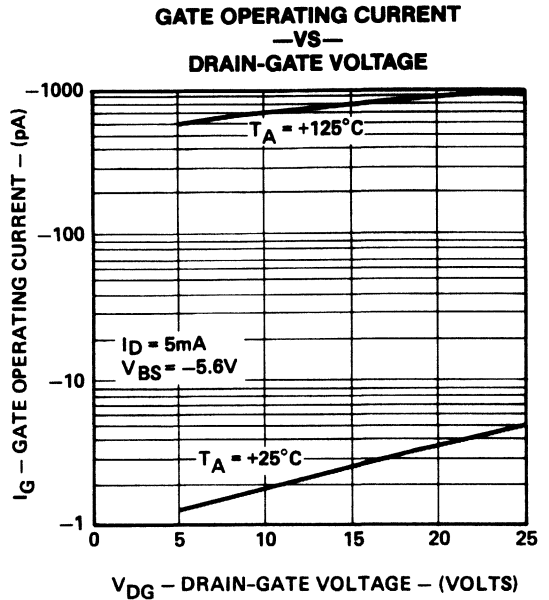
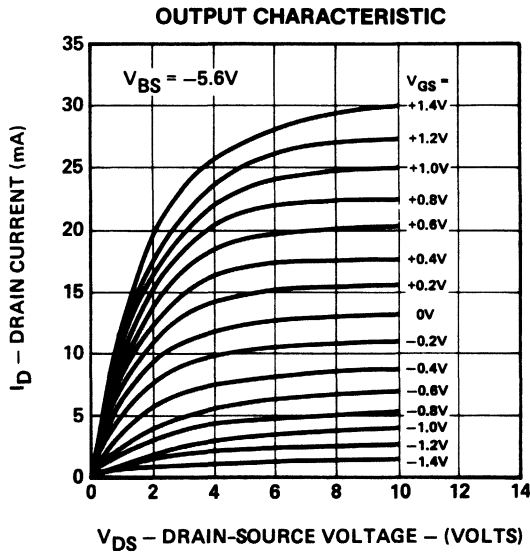
V_{out} max.—+20V

Input Bias Current—100 pA max., 4 pA typ.

Differential Input Bias Current—0.4 pA typ.

Gate Voltages must be positive with respect to Body (Substrate) Voltage at all times.

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$, per side, unless otherwise specified)



N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION

TO-226AA (TO-92) Plastic Package	VN0104N3	VN0106N3	VN0109N3
Sorted Chips in Waffle Pack	VN0104ND	VN0106ND	VN0109ND
Description	40V, 3.0 ohm	60V, 5.0 ohm	90V, 5.0 ohm

FEATURES

- Gate Standoff Voltage, $\pm 40V$ min
- Low Output and Transfer Capacitances
- Extended Safe Operating Area
- Complementary P-Channel Devices Available

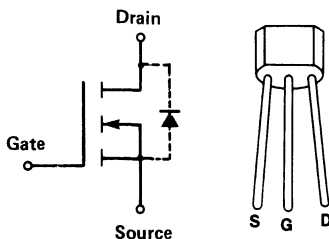
APPLICATIONS

- Complementary Voltage and Current Drivers
- Line Drivers
- Pulse Amplifiers
- Solid-State Relays

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ C$ unless otherwise specified)

Drain-Source Voltage			
VN0104	+ 40V	
VN0106	+ 60V	
VN0109	+ 90V	
Drain-Gate Voltage ($V_{GS} = 0$)			
VN0104	+ 40V	
VN0106	+ 60V	
VN0109	+ 90V	
Gate-Source Voltage	$\pm 40V$	
Continuous Drain Current			
	$T_A = +25^\circ C$	$T_C = +25^\circ C$	
TO-92(N3)pkg.	.23A	.42A	
Peak Pulsed Drain Current	+ 2.0A	
Continuous Device Dissipation			
	$T_A = +25^\circ C$	$T_C = +25^\circ C$	
TO-92(N3)pkg.	0.30W	1.0W	
Linear Derating Factor			
	$T_A = +25^\circ C$	$T_C = +25^\circ C$	
TO-92(N3)pkg.	3.0mW/ $^\circ C$	10mW/ $^\circ C$	
Operating Junction and Storage Temperature Range	$-55^\circ C$ to + 150 $^\circ C$	
Lead Temperature (1/16" from mounting surface for 30 sec.)	+ 260 $^\circ C$	

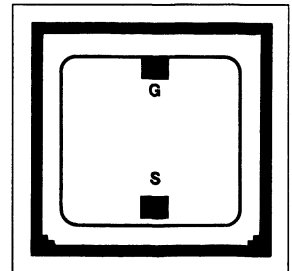
PIN CONFIGURATION



PACKAGE DIMENSIONS (TO-92) TO-226A

(See Package 5)

CHIP CONFIGURATION



Dimensions: .054 x .051 x .020 in.
Drain is backside contact.

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

#	PARAMETER	VN0104			VN0106			VN0109			UNIT	TEST CONDITIONS		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX				
1	BV_{DSS} Drain-Source Breakdown Voltage	40	60		60	90		90	105		V	$I_D = 1.0\text{mA}$, $V_{GS} = 0$		
2	I_{DSS} Drain-Source Off Leakage Current			100							μA	$V_{DS} = 32\text{V}$	$T_A = +125^\circ\text{C}$	
3									100			$V_{DS} = 48\text{V}$		
4										100				$V_{DS} = 72\text{V}$
5			.01	1.0									$V_{DS} = 40\text{V}$	$V_{GS} = 0$
6						.01	1.0						$V_{DS} = 60\text{V}$	
7									.01	1.0			$V_{DS} = 90\text{V}$	
8		I_{GBS} Gate-Body Leakage Current			± 1.0			± 1.0				± 1.0	μA	$V_{GB} = \pm 40\text{V}$
9				± 10			± 10			± 10	nA	$V_{GB} = \pm 20\text{V}$		
10	$V_{GS(th)}$ Gate-Source Threshold Voltage	0.8		2.4	0.8		2.4	0.8		2.4	V	$V_{DS} = V_{GS}$, $I_D = 1.0\text{mA}$		
11	$r_{DS(on)}$ Drain-Source On Resistance			5.0			5.0			5.0	ohms	$V_{GS} = 5\text{V}$, $I_D = .25\text{A}$	(Note 1)	
12				3.0			3.0			3.0		$V_{GS} = 10\text{V}$, $I_D = 1.0\text{A}$		
13	$I_{D(on)}$ On Drain Current	.75		.75			.75			.75	A	$V_{GS} = 5\text{V}$		$V_{DS} = 25\text{V}$
14		2.0		2.0			2.0			2.0		$V_{GS} = 10\text{V}$		
15	θ_{rs} Common-Source Forward Transcond.	300			300			300			mmhos	$V_{DS} = 25\text{V}$, $I_D = 0.5\text{A}$		
16	V_{SD} Source-Drain Forward Voltage			1.8			1.8			1.8	V	$I_{SD} = 1.0\text{A}$, $V_{GS} = 0$		
17	C_{iss} Common-Source Input Capacitance			60			60			60	pF	$V_{DS} = 25\text{V}$ $V_{GS} = 0$ $f = 1\text{MHz}$		
18	C_{oss} Common-Source Output Capacitance		11	25		11	25		11	25				
19	C_{rss} Common-Source Reverse Transfer Capacitance		1.5	5.0		1.5	5.0		1.5	5.0				
20	t_{on} Turn ON Time		8.0	13		8.0	13		8.0	13	nS	$V_{DD} = 25\text{V}$, $V_{G(on)} = 10\text{V}$		
21	t_{off} Turn OFF Time		8.0	17		8.0	17		8.0	17		$R_G = 51\Omega$, $R_L = 25\Omega$		

NOTE 1: Pulse Test, 80 μ Sec, 1% Duty Cycle

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION

TO-92 Plastic Package	VN0610LL	VN2222LL
Description	80V, 500m	80V, 7.50m

FEATURES

- High Gate Oxide Breakdown, $\pm 40V$ min.
- Low Output and Transfer Capacitances
- Extended Safe Operating Area

APPLICATIONS

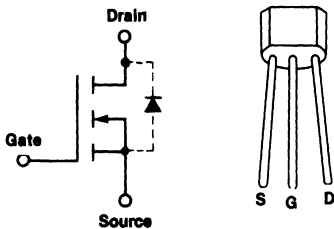
- High-Speed Pulse Amplifiers
- Logic Buffers
- Line Drivers
- Solid-State Relays
- Motor Controls
- Power Supplies

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ C$ unless otherwise noted)

Drain-Source Voltage	+60V	
Drain-Gate Voltage ($V_{GS} = 0$)	+60V	
Gate-Source Voltage	$\pm 40V$	
Continuous Drain Current	$T_A = 25^\circ C$	$T_C = 25^\circ C$
	VN0610LL .18A	.32A
	VN2222LL .15A	.26A
Peak Pulsed Drain Current	1.0A	

Continuous Device Dissipation	$T_A = +25^\circ C$	$T_C = +25^\circ C$	
	0.30	1.0	W
Linear Derating Factor	$T_A = +25^\circ C$	$T_C = +25^\circ C$	
	2.4	8.0	mW/ $^\circ C$
Operating Junction Temperature Range	-55 to +150 $^\circ C$		
Storage Temperature Range	-55 to +150 $^\circ C$		
Lead Temperature (1/16" from mounting surface for 30 Sec)	+260 $^\circ C$		

SCHEMATIC DIAGRAM/PACKAGE



PACKAGE DIMENSIONS (TO-92) TO-226AA

(See Package 5)

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTICS		VN0610LL			VN2222LL			UNIT	TEST CONDITIONS
			MIN	TYP	MAX	MIN	TYP	MAX		
1	STATIC	BV_{DSS} Drain-Source Breakdown Voltage	60	100		60	100		V	$I_D = 100\mu\text{A}, V_{GS} = 0$
2		$V_{GS(th)}$ Gate-Source Threshold Voltage	0.8	1.9	2.5	0.6	1.9	2.5	V	$I_D = 1.0\text{mA}, V_{DS} = V_{GS}$
3		I_{GBS} Gate-Body Leakage Current		± 1.0	± 100		± 1.0	± 100	nA	$V_{GS} = \pm 30\text{V}, V_{DS} = 0$
4		I_{DSS} Drain-Source OFF Leakage Current		0.1	10		0.1	10	μA	$V_{DS} = 48\text{V}, V_{GS} = 0$
5				5.0	500		5.0	500		
6		$I_{D(on)}$ ON Drain Current	1.0	2.2		1.0	2.2		A	$V_{DS} = 10\text{V}, V_{GS} = 10\text{V}$ (Note 1)
7		$V_{DS(on)}$ Drain-Source ON Voltage		0.9	1.5		0.9	1.5	V	$V_{GS} = 5\text{V}, I_D = 0.2\text{A}$ (Note 1)
8				1.5	2.5		1.5	3.75		$V_{GS} = 10\text{V}, I_D = 0.5\text{A}$ (Note 1)
9		$r_{DS(on)}$ Drain-Source ON Resistance		4.5	7.5		4.5	7.5	ohms	$V_{GS} = 5\text{V}, I_D = 0.2\text{A}$ (Note 1)
10				3.0	5.0		3.0	7.5		$V_{GS} = 10\text{V}, I_D = 0.5\text{A}$ (Note 1)
11				4.7	9.0		4.7	13.5		$T_A = +125^\circ\text{C}$
12	DYNAMIC	g_{fs} Common-Source Forward Transcond.	100	400		100	400		mmhos	$V_{DS} = 10\text{V}, I_D = 0.5\text{A}$ $f = 1\text{KHz}$ (Note 1)
13		C_{iss} Common-Source Input Capacitance		80	100		80	100	pF	$V_{DS} = 15\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$
14		C_{rse} Common-Source Reverse Transfer Capacitance		1.3	5.0		1.3	5.0		
15		C_{oss} Common-Source Output Capacitance		10.5	25		10.5	25		
16		t_{on} Turn-On Time		5.0	10		5.0	10	nSec	$V_{DD} = 15\text{V}, V_{GS(on)} = 10\text{V}$ $R_G = 25\Omega, R_L = 25\Omega$
17		t_{off} Turn-Off Time		6.0	10		6.0	10		

Note 1: Pulse Test 80 μSec , 1% Duty Cycle

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION

TO-92 Plastic Package	QUT	VN10KN3
Description		60V, 5 ohm

FEATURES

- High Gate Oxide Breakdown, $\pm 40V$ min.
- Low Output and Transfer Capacitances
- Extended Safe Operating Area

APPLICATIONS

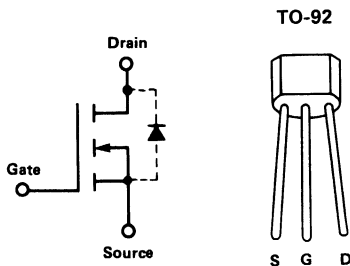
- High-Speed Pulse Amplifiers
- Logic Buffers
- Line Drivers
- Solid-State Relays
- Motor Controls
- Power Supplies

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ C$ unless otherwise noted)

Drain-Source Voltage	+60V	
Drain-Gate Voltage ($V_{GS} = 0$)	+60V	
Gate-Source Voltage	$\pm 30V$	
Continuous Drain Current	$T_A = 25^\circ C$	$T_C = 25^\circ C$
	.24A	.32A
Peak Pulsed Drain Current	1.0A	

Continuous Device Dissipation	$T_A = +25^\circ C$	$T_C = +25^\circ C$	
	0.30	1.0	W
Linear Derating Factor	$T_A = +25^\circ C$	$T_C = +25^\circ C$	
	2.4	8.0	mW/ $^\circ C$
Operating Junction Temperature Range	-55 to +150 $^\circ C$		
Storage Temperature Range	-55 to +150 $^\circ C$		
Lead Temperature (1/16" from mounting surface for 30 Sec)	+260 $^\circ C$		

SCHEMATIC DIAGRAM/PACKAGE



PACKAGE DIMENSIONS (TO-92) TO-226AA

(See Package 5)

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC		VN10KN			UNIT	TEST CONDITIONS
			MIN	TYP	MAX		
1	STATIC	BV_{DSS} Drain-Source Breakdown Voltage	60	100		V	$I_D = 100\mu\text{A}, V_{GS} = 0$
2		$V_{GS(th)}$ Gate-Source Threshold Voltage	0.8	1.9	2.5	V	$I_D = 1.0\text{mA}, V_{DS} = V_{GS}$
3		I_{GBS} Gate-Body Leakage Current		± 1.0	± 100	nA	$V_{GS} = \pm 15\text{V}, V_{DS} = 0$
4		I_{DSS} Drain-Source OFF Leakage Current		0.1	10	μA	$V_{DS} = 40\text{V}, V_{GS} = 0$ $T_A = 125^\circ\text{C}$
5				5.0	500		
6		$I_{D(on)}$ ON Drain Current		0.25		A	$V_{GS} = 5\text{V}, V_{DS} = 10\text{V}$
7				0.75			$V_{GS} = 10\text{V}$ (Note 1)
8		$V_{DS(on)}$ Drain-Source ON Voltage		1.5	2.5	V	$V_{GS} = 10\text{V}, I_D = 0.5\text{A}$ (Note 1)
9				3.0	5.0	ohms	$V_{GS} = 10\text{V}, I_D = 0.5\text{A}$ (Note 1)
10			$r_{DS(on)}$ Drain-Source ON Resistance		4.7	9.0	
11	DYNAMIC	g_{fs} Common-Source Forward Transcond.	100	400		mmhos	$V_{DS} = 10\text{V}, I_D = 0.5\text{A}$ $f = 1\text{KHz}$ (Note 1)
12		C_{iss} Common-Source Input Capacitance		80	100	pF	$V_{DS} = 15\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$
13		C_{rss} Common-Source Reverse Transfer Capacitance		1.3	5.0		
14		C_{oss} Common-Source Output Capacitance		10.5	25		
15		t_{on} Turn-On Time		5.0	10	nSec	$V_{DD} = V_{G(on)} = 10\text{V}$ $R_G = 25\Omega, R_L = 25\Omega$
16		t_{off} Turn-Off Time		6.0	10		

Note 1: Pulse Test $80\mu\text{Sec}$, 1% Duty Cycle

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION

TO-237 Plastic Package	VN10LM	VN222LM
Description	60V, 5 ohm	60V, 7.5 ohm

FEATURES

- High Gate Oxide Breakdown, $\pm 40V$ min.
- Low Output and Transfer Capacitances
- Extended Safe Operating Area

APPLICATIONS

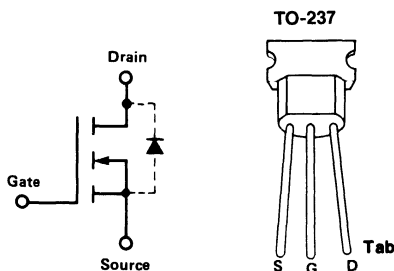
- High-Speed Pulse Amplifiers
- Logic Buffers
- Line Drivers
- Solid-State Relays
- Motor Controls
- Power Supplies

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ C$ unless otherwise noted)

Drain-Source Voltage	+60V	
Drain-Gate Voltage ($V_{GS} = 0$)	+60V	
Gate-Source Voltage	± 40	
Continuous Drain Current	$T_A = 25^\circ C$	$T_C = 25^\circ C$
VN10LM	.19A	.44A
VN222LM	.16A	.36A
Peak Pulsed Drain Current	1.0A	

Continuous Device Dissipation	$T_A = +25^\circ C$	$T_C = +25^\circ C$	
	0.36	1.8	W
Linear Derating Factor	$T_A = +25^\circ C$	$T_C = +25^\circ C$	
	2.9	14.4	mW/ $^\circ C$
Operating Junction Temperature Range	-55 to +150 $^\circ C$		
Storage Temperature Range	-55 to +150 $^\circ C$		
Lead Temperature (1/16" from mounting surface for 30 Sec)	+260 $^\circ C$		

SCHEMATIC DIAGRAM/PACKAGE



PACKAGE DIMENSIONS

TO-237
(See Package 7)

N-CHANNEL ENHANCEMENT-MODE D-MOS FET

ORDERING INFORMATION

Sorted Chips in Wafer Pack	VN2410CHP
TO-226AA (TO-92) Plastic Package	VN2410L
TO-226AA (TO-92) Plastic Package	VN2410M
TO-226AA (TO-92) Plastic Package	VN2410M
TO-226AA (TO-92) Plastic Package	VN2410M

FEATURES

- Gate Stand-off Voltage, $\pm 40V$ min.

APPLICATIONS

- Motor Controls
- Line Drivers
- Power Supplies

ABSOLUTE MAXIMUM RATINGS ($T_C = +25^\circ C$ unless otherwise noted)

Drain-Source Voltage	240V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	240V
Gate-Source Voltage	$\pm 40V$
Continuous Drain Current	

	$T_C = +100^\circ C$	$T_C = +25^\circ C$
VN2410L	0.14	0.23
VN2410M	0.16	0.26

Peak Pulsed Drain Current 1.0A

Maximum Power Dissipation

	$T_C = +100^\circ C$	$T_C = +25^\circ C$
VN2410L	0.5W	1.35W
VN2410M	0.7W	1.90W

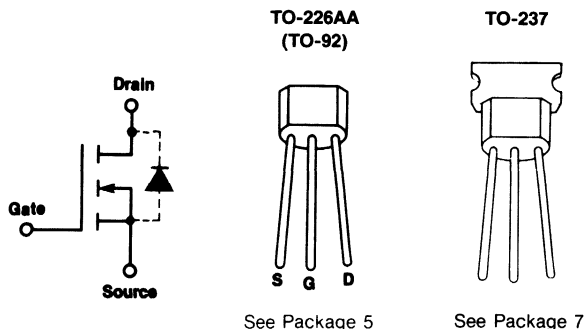
Linear Derating Factor

	Junction to Ambient ($mW/^\circ C$)	Junction to Case ($mW/^\circ C$)
VN2410L	6.66	10.8
VN2410M	9.33	14.4

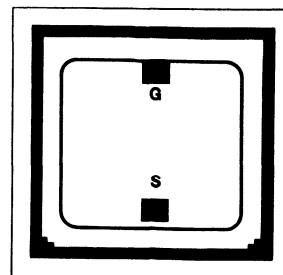
Operating Junction and Storage

Temperature Range	-55 to $+150^\circ C$
Lead Temperature ($1/16''$ from mounting surface for 10 Sec)	$+260^\circ C$

PIN CONFIGURATION



CHIP CONFIGURATION



Dimensions: $.054 \times .051 \times .020$ in.
Drain is backside contact.

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC		VN10LM			VN222LM			UNIT	TEST CONDITIONS	
			MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS} Drain-Source Breakdown Voltage	60	100		60	100		V	$I_D = 100\mu\text{A}$, $V_{GS} = 0$	
2		$V_{GS(th)}$ Gate-Source	0.8	1.9	2.5	0.6	1.9	2.5	V	$I_D = 1.0\text{mA}$, $V_{DS} = V_{GS}$	
3		I_{GBS} Gate-Body Leakage Current		± 1.0	± 100		± 1.0	± 100	nA	$V_{GS} = \pm 30\text{V}$, $V_{DS} = 0$	
4		I_{DSS} Drain-Source OFF Leakage Current		0.1	10		0.1	10	μA	$V_{DS} = 48\text{V}$, $V_{GS} = 0$	
5				5.0	500		5.0	500			$T_A = 125^\circ\text{C}$
6		$I_{D(on)}$ ON Drain Current	1.0	2.2		1.0	2.2		A	$V_{DS} = 10\text{V}$, $V_{GS} = 10\text{V}$ (Note 1)	
7		$V_{DS(on)}$ Drain-Source ON Voltage		0.9	1.5		0.9	1.5	V	$V_{GS} = 5\text{V}$, $I_D = 0.2\text{A}$ (Note 1)	
8				1.5	2.5		1.5	3.75			$V_{GS} = 10\text{V}$, $I_D = 0.5\text{A}$ (Note 1)
9		$r_{DS(on)}$ Drain-Source ON Resistance		4.5	7.5		4.5	7.5	ohms	$V_{GS} = 5\text{V}$, $I_D = 0.2\text{A}$ (Note 1)	
10				3.0	5.0		3.0	7.5			$V_{GS} = 10\text{V}$, $I_D = 0.5\text{A}$ (Note 1)
11				4.7	9.0		4.7	13.5			$T_A = +125^\circ\text{C}$
12	DYNAMIC	g_{fs} Common-Source Forward Transcond.	100	400		100	400		mmhos	$V_{DS} = 10\text{V}$, $I_D = 0.5\text{A}$ $f = 1\text{KHz}$ (Note 1)	
13		C_{iss} Common-Source Input Capacitance		80	100		80	100	pF	$V_{DS} = 15\text{V}$, $V_{GS} = 0$ $f = 1\text{MHz}$	
14		C_{rbs} Common-Source Reverse Transfer Capacitance		1.3	5.0		1.3	5.0			
15		C_{oss} Common-Source Output Capacitance		10.5	25		10.5	25			
16		t_{on} Turn-On Time		5.0	10		5.0	10	nSec	$V_{DD} = 15\text{V}$, $V_{G(on)} = 10\text{V}$ $R_G = 25\Omega$, $R_L = 25\Omega$	
17		t_{off} Turn-Off Time		6.0	10		6.0	10			

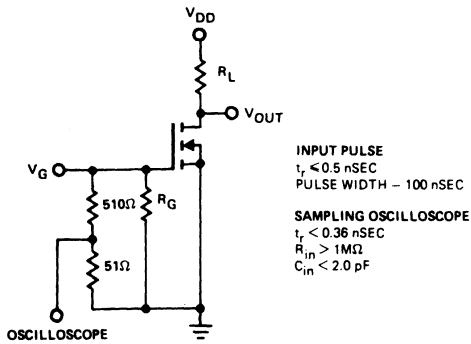
Note 1: Pulse Test 80 μ Sec, 1% Duty Cycle

ELECTRICAL CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise noted)

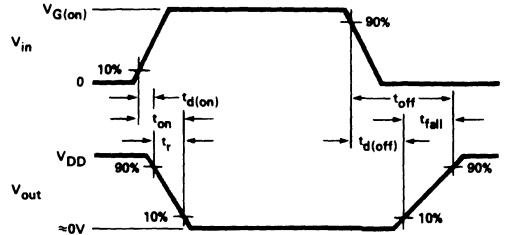
#	CHARACTERISTIC	VN2410			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
1	BV_{DSS} Drain-Source Breakdown Voltage	240	290		V	$I_D = 250\mu\text{A}, V_{GS} = 0$
2	$V_{GS(th)}$ Gate-Source Threshold Voltage	1.0	1.3	2.0	V	$V_{DS} = V_{GS}$ $I_D = 1\text{mA}$ $T_C = +125^\circ\text{C}$
3		0.4				
4	I_{GBS} Gate-Body Leakage Current			100	nA	$V_{GS} = 15\text{V}, V_{DS} = 0$ $T_C = +125^\circ\text{C}$ $V_{GS} = -15\text{V}, V_{DS} = 0$
5				500		
6				-100		
7	I_{DSS} Drain-Source OFF Leakage Current			10	μA	$V_{DS} = 120\text{V}$ $V_{GS} = 0$ $T_C = +125^\circ\text{C}$
8				500		
9	$I_{D(on)}$ ON Drain Current ⁽¹⁾	1.0	1.3		A	$V_{DS} = 25\text{V}, V_{GS} = 10\text{V}$
10	$V_{DS(on)}$ Drain-Source ⁽¹⁾ ON Voltage		0.7	1.0	V	$V_{GS} = 2.5\text{V}, I_D = 0.1\text{A}$ $V_{GS} = 10\text{V}, I_D = 0.5\text{A}$
11				3.9		
12	$r_{DS(on)}$ Drain-Source ⁽¹⁾ ON Resistance		7.8	10	ohms	$V_{GS} = 10\text{V}$ $I_D = 0.5\text{A}$ $T_C = +125^\circ\text{C}$ $V_{GS} = 2.5\text{V}, I_D = 0.1\text{A}$
13				24.7		
14				7.0		
15	g_{fs} Common-Source ⁽¹⁾ Forward Transcond.	0.3	0.75		S	$V_{DS} = 25\text{V}, I_D = 0.5\text{A}, f = 1\text{KHz}$
16	C_{iss} Common-Source Input Capacitance			125	pF	$V_{DS} = 25\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$
17	C_{rss} Common-Source Reverse Transfer Capacitance		6.0	20		
18	C_{oss} Common-Source Output Capacitance		15	50		
19	$t_{d(on)}$ Turn-ON Delay Time			8.0	nsec	$V_{DD} = 60\text{V}$ $R_L = 600\text{ohms}$ $R_G = 25\text{ohms}$ $V_{G(on)} = 10\text{V}$
20	t_r Rise Time			8.0		
21	$t_{d(off)}$ Turn-OFF Delay Time			23		
22	t_f Fall Time			24		
23	I_S Continuous Source Current	.14			A	
24	I_{SM} Peak Source Current ⁽¹⁾	1.0				
25	V_{SD} Source-Drain ⁽¹⁾ Forward Voltage		-1.2			

Note 1: Pulse test 80 μSec , 1% Duty Cycle

SWITCHING TIMES TEST CIRCUIT

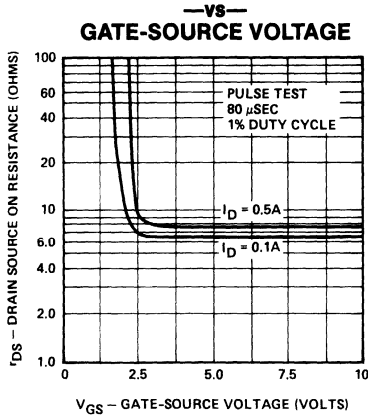


TEST WAVEFORMS

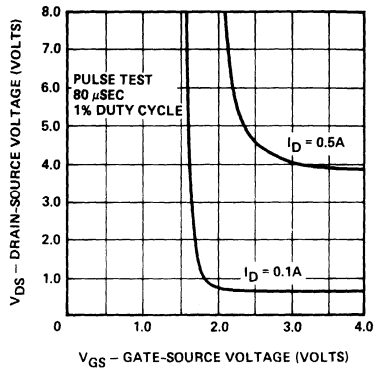


TYPICAL PERFORMANCE CHARACTERISTICS ($T_c = +25^\circ\text{C}$ unless otherwise noted)

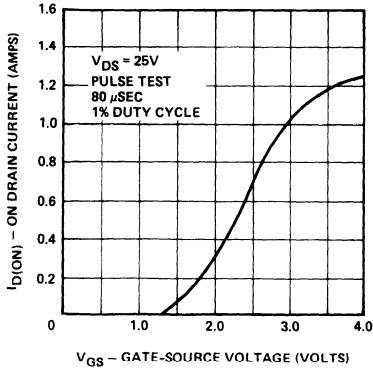
DRAIN-SOURCE ON RESISTANCE



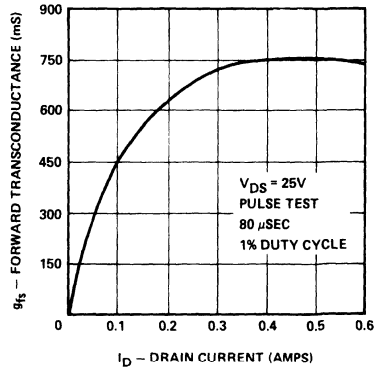
ON VOLTAGE CHARACTERISTICS



ON DRAIN CURRENT
—vs—
GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE
—vs—
ON DRAIN CURRENT



P-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION

TO-92(N3) Pkg. Part No.	VPO104N3	VPO106N3	VPO109N3
Part No.	VPO104	VPO106	VPO109
Drain-Source Voltage	40V	60V	90V

FEATURES

- Gate Standoff Voltage, $\pm 40V$ min
- Low Output and Transfer Capacitances
- Extended Safe Operating Area
- Complementary N-Channel Devices Available

APPLICATIONS

- Complementary Voltage and Current Drivers
- Line Drivers
- Pulse Amplifiers
- Solid-State Relays

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ C$ unless otherwise specified)

Drain-Source Voltage

VPO104	-40V
VPO106	-60V
VPO109	-90V

Drain-Gate Voltage ($V_{GS} = 0$)

VPO104	-40V
VPO106	-60V
VPO109	-90V

Gate-Source Voltage

	$\pm 40V$
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Continuous Drain Current

	$T_A = +25^\circ C$	$T_C = +25^\circ C$
TO-92(N3)pkg.	-0.14A	-0.26A

Peak Pulsed Drain Current

	-0.5A
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Continuous Device Dissipation

	$T_A = +25^\circ C$	$T_C = +25^\circ C$
TO-92(N3)pkg.	0.30W	1.0W

Linear Derating Factor

	$T_A = +25^\circ C$	$T_C = +25^\circ C$
TO-92(N3)pkg.	3.0mW/ $^\circ C$	10mW/ $^\circ C$

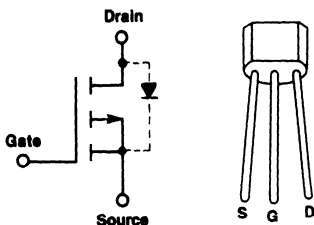
Operating Junction and Storage Temperature

Range	-55 $^\circ C$ to +150 $^\circ C$
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Lead Temperature (1/16" from mounting surface

for 30 sec.)	+260 $^\circ C$
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PIN CONFIGURATION

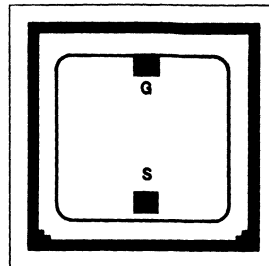


PACKAGE DIMENSIONS (TO-92) TO-226A

(See Package 5)

All dimensions in inches and (millimeters)

CHIP CONFIGURATION



Dimensions: .054 x .051 x .020 in.
Drain is backside contact.

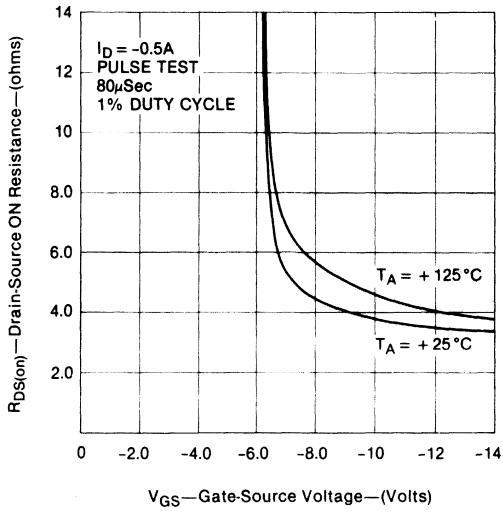
ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)

#	PARAMETER	VP0104			VP0106			VP0109			UNIT	CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	BV _{DSS} Drain-Source Breakdown Voltage	-40	-60		-60	-90		-90	-105		V	I _D = -1.0mA, V _{GS} = 0	
2	I _{DSS} Drain-Source Off Leakage Current			-1.0							mA	V _{DS} = -32V	T _A = +125°C
3							-1.0					V _{DS} = -48V	
4										-1.0		V _{DS} = -72V	V _{GS} = 0
5				-0.01	-10							V _{DS} = -40V	V _{GS} = 0
6						-0.01	-10					V _{DS} = -60V	
7									-0.01	-10		V _{DS} = -90V	
8		I _{GBS} Gate-Body Leakage Current			± 1.0			± 1.0			± 1.0	µA	V _{GB} = ± 40V
9				± 10			± 10			± 10	nA	V _{GB} = ± 20V	
10	V _{GS(th)} Gate-Source Threshold Voltage	-1.5		-3.5	-1.5		-3.5	-1.5		-3.5	V	V _{DS} = V _{GS} , I _D = -1.0mA	
11	r _{DS(on)} Drain-Source On Resistance		10	15		10	15		10	15	ohms	V _{GS} = -5V, I _D = -0.1A	(Note 1)
12			4.0	8.0		4.0	8.0		4.0	8.0		V _{GS} = -10V, I _D = -0.5A	
13	I _{D(on)} On Drain Current	-0.1	-0.2		-0.1	-0.2		-0.1	-0.2		A	V _{GS} = -5V	
14		-0.5	-1.2		-0.5	-1.2		-0.5	-1.2			V _{GS} = -10V	
15	g _{fs} Common-Source Forward Transcond.	150	275		150	275		150	275		mmhos	V _{DS} = -25V, I _D = -0.5A	
16	V _{SD} Source-Drain Forward Voltage			-2.0			-2.0			-2.0	V	I _{SD} = -1.0A, V _{GS} = 0	
17	C _{iSS} Common-Source Input Capacitance			60			60			60	pF	V _{DS} = -25V V _{GS} = 0 f = 1MHz	
18	C _{oss} Common-Source Output Capacitance		11	30		11	30		11	30			
19	C _{rSS} Common-Source Reverse Transfer Capacitance		1.5	8.0		1.5	8.0		1.5	8.0			
20	t _{on} Turn ON Time		8.0	16		8.0	16		8.0	16	nS	V _{DD} = -25V, V _{GS(on)} = -10V	
21	t _{off} Turn OFF Time		8.0	15		8.0	15		8.0	15		R _G = 51Ω, R _L = 51Ω	

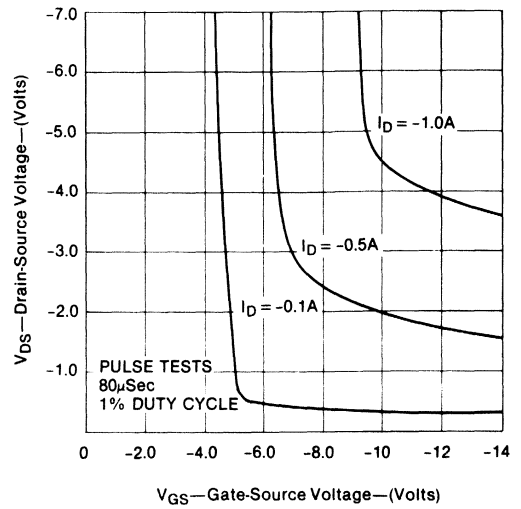
NOTE 1: Pulse Test, 80µSec, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

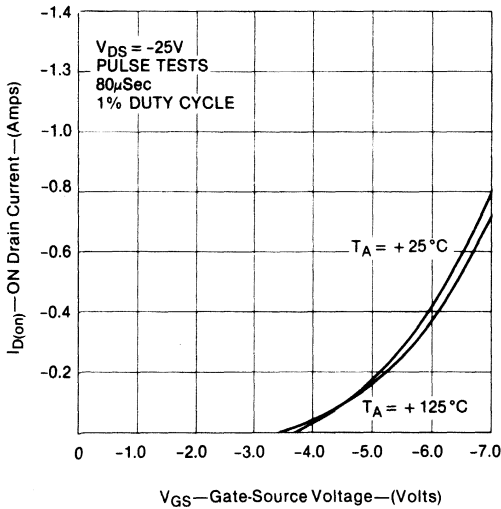
DRAIN-SOURCE ON RESISTANCE
—VS—
GATE-SOURCE VOLTAGE



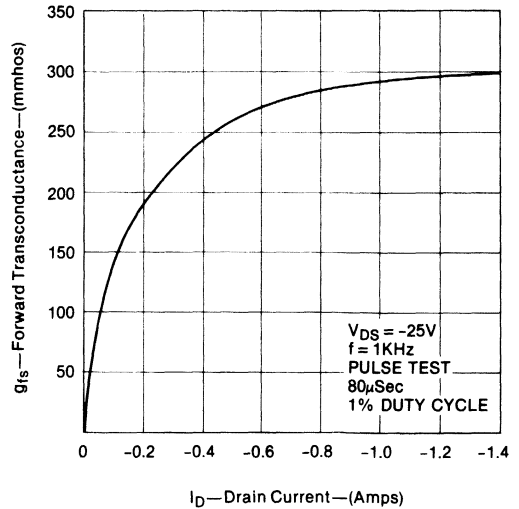
ON VOLTAGE CHARACTERISTICS



ON DRAIN CURRENT
—VS—
GATE SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE
—VS—
ON DRAIN CURRENT



P-CHANNEL ENHANCEMENT-MODE D-MOS FETs

ORDERING INFORMATION

Sorted Chips in Wafer Pack	VP0535ND	VP0540ND
TO-92 Plastic Package	VP0535N	VP0540N
Description	-350V, 75Ω	-400V, 75Ω

FEATURES

- Gate Stand-off Voltage, ±40V min.
- Low Output and Transfer Capacitances
- N-Channel Complements Available
- High Drain-Source Breakdown

APPLICATIONS

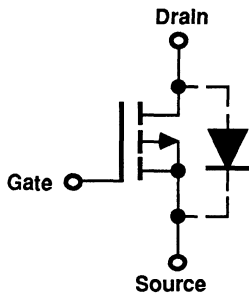
- Motor Controls
- Logic Interfaces
- Pulse Amplifiers
- Level Translators

ABSOLUTE MAXIMUM RATINGS ($T_c = +25^\circ\text{C}$ unless otherwise noted)

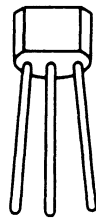
Drain-Source Voltage		
VP0535	-350V
VP0540	-400V
Drain-Gate Voltage ($R_{GS} = 1\text{M}\Omega$)		
VP0535	-350V
VP0540	-400V
Gate-Source Voltage		±40V
Continuous Drain Current		
	$T_c = +100^\circ\text{C}$	$T_c = -25^\circ\text{C}$
TO-92 Pkg.	-0.05A
		-0.14A
Peak Pulsed Drain Current	-0.2A

Maximum Power Dissipation		
	$T_c = +100^\circ\text{C}$	$T_c = +25^\circ\text{C}$
TO-92 Pkg.	0.4W
		3.0W
Linear Derating Factor		
	Junction to Ambient	Junction to Case
	(mW/°C)	(mW/°C)
TO-92 Pkg.	3.0
		24
Operating Junction and Storage		
Temperature Range	-55 to +150°C
Lead Temperature (1/16" from mounting surface for 10 Sec)	+300°C

PIN CONFIGURATION

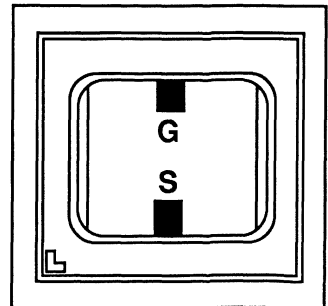


TO-226A (TO-92)



See Package 5

CHIP CONFIGURATION



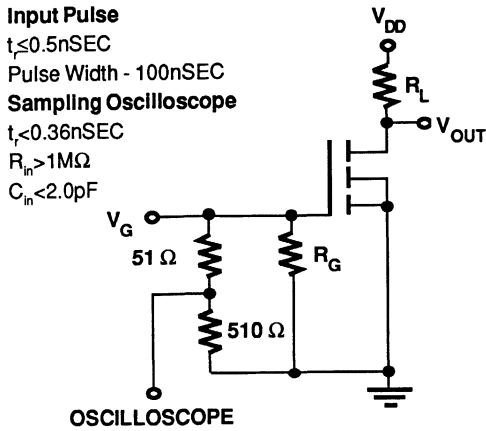
Dimensions: 0.054 x 0.051 x 0.020 inches
Drain is backside contact

ELECTRICAL CHARACTERISTICS ($T_c = +25^\circ\text{C}$ unless otherwise noted)

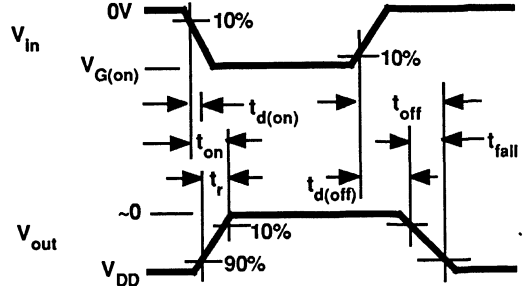
#	CHARACTERISTICS		VP0535			VP0540			UNIT	TEST CONDITIONS		
			MIN	TYP	MAX	MIN	TYP	MAX				
1	STATIC	BV_{DS} Drain-Source Breakdown Voltage	-350			-400			V	$I_D = -1.0\text{mA}, V_{GS} = 0$		
2		$V_{GS(th)}$ Gate-Source Threshold Voltage	-2.0		-4.5	-2.0		-4.5	V	$V_{DS} = V_{GS}$ $I_D = -1.0\text{mA}$		
3		I_{GBS} Gate-Body Leakage Current			-100			-100	nA	$V_{GS} = -30\text{V}, V_{DS} = 0$		
4		I_{GBS} Gate-Body Leakage Current			100			100	nA	$V_{GS} = +30\text{V}, V_{DS} = 0$		
5		I_{DSS} Drain-Source OFF Leakage Current	I_{DSS} Drain-Source OFF Leakage Current		-0.1	-10				μA	$V_{DS} = -350\text{V}$ $V_{GS} = 0$	
6			I_{DSS} Drain-Source OFF Leakage Current		-0.3	-500					$V_{DS} = -280\text{V}$ $V_{GS} = 0$ $T_c = +125^\circ\text{C}$	
7			I_{DSS} Drain-Source OFF Leakage Current				-0.1	-10			$V_{DS} = -400\text{V}$ $V_{GS} = 0$	
8			I_{DSS} Drain-Source OFF Leakage Current				-0.3	-500			$V_{DS} = -320\text{V}$ $V_{GS} = 0$ $T_c = +125^\circ\text{C}$	
9	$I_{D(on)}$ ON Drain Current(1)	$I_{D(on)}$ ON Drain Current(1)	-25	-120		-25	-120		mA	$V_{DS} = -25\text{V}$ $V_{GS} = -5\text{V}$		
10		$I_{D(on)}$ ON Drain Current(1)	-200	-400		-200	-400			$V_{GS} = -10\text{V}$		
11		$r_{DS(on)}$ Drain-Source(1) ON Resistance	$r_{DS(on)}$ Drain-Source(1) ON Resistance		55	100		55		100	ohms	$V_{GS} = -5\text{V}$ $I_D = -10\text{mA}$ $T_c = +125^\circ\text{C}$
12			$r_{DS(on)}$ Drain-Source(1) ON Resistance		78	170		78		170		$V_{GS} = -10\text{V}$ $I_D = -50\text{mA}$ $T_c = +125^\circ\text{C}$
13	$r_{DS(on)}$ Drain-Source(1) ON Resistance			48	75		48	75	$V_{GS} = -10\text{V}$ $I_D = -50\text{mA}$ $T_c = +125^\circ\text{C}$			
14	$r_{DS(on)}$ Drain-Source(1) ON Resistance		73	125		73	125		$V_{GS} = -10\text{V}$ $I_D = -50\text{mA}$ $T_c = +125^\circ\text{C}$			
15	DYNAMIC	g_{fs} Common-Source(1) Forward Transcond.	50	110		50	100		mS	$V_{DS} = -25\text{V}, I_D = -50\text{mA}$, $f = 1\text{KHz}$		
16		C_{iss} Common-Source Input Capacitance			60			60	pF	$V_{DS} = -25\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$		
17		C_{rss} Common-Source Reverse Transfer Capacitance			5.0			5.0				
18		C_{oss} Common-Source Output Capacitance			20			20				
19	$t_{(on)}$ Turn-ON Delay Time			10			10	nsec		$V_{DD} = -25\text{V}$ $R_L = 100\Omega$ $R_G = 51\Omega$ $V_{GS(on)} = -10\text{V}$		
20	t_r Rise Time			15			15					
21	$t_{(off)}$ Turn-OFF Delay Time			15			15					
22	t_f Fall Time			10			10					
23	DIODE	I_S Continuous Source Current	-0.05			-0.05			A			
24		I_{SM} Peak Source Current(1)			-0.2			-0.2				
25		V_{DS} Source-Drain(1) Forward Voltage		1.2			1.2			V	$V_{GS} = 0, I = .14\text{A}$	

Note 1: Pulse Test 80 μSec , 1% Duty Cycle

SWITCHING TIMES TEST CIRCUIT

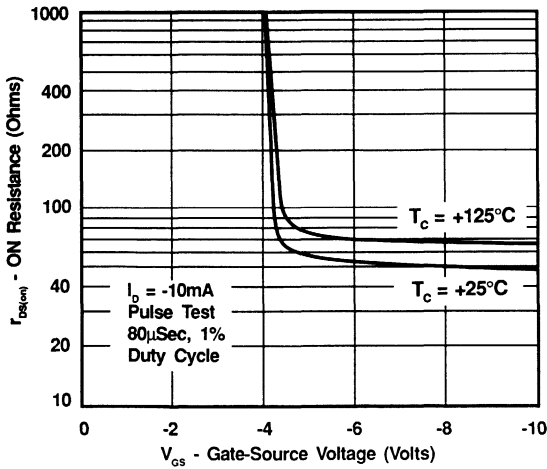


TEST WAVEFORMS

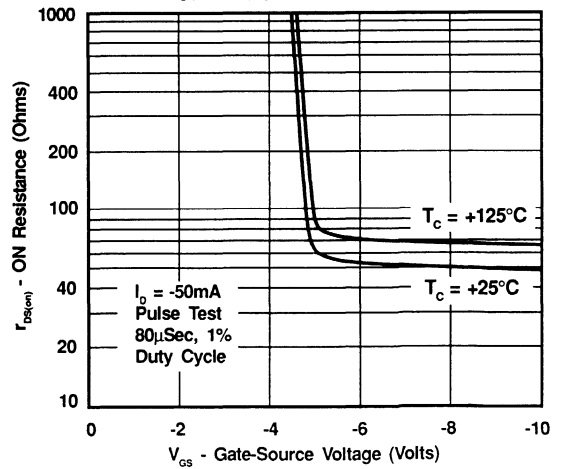


TYPICAL PERFORMANCE CHARACTERISTICS ($T_c = +25^\circ\text{C}$ unless otherwise noted)

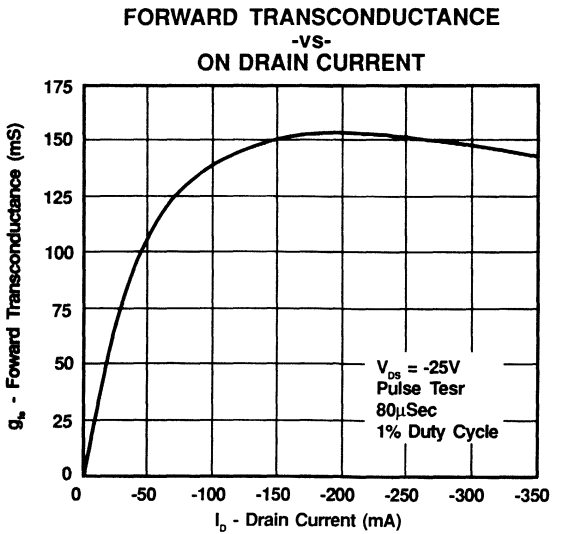
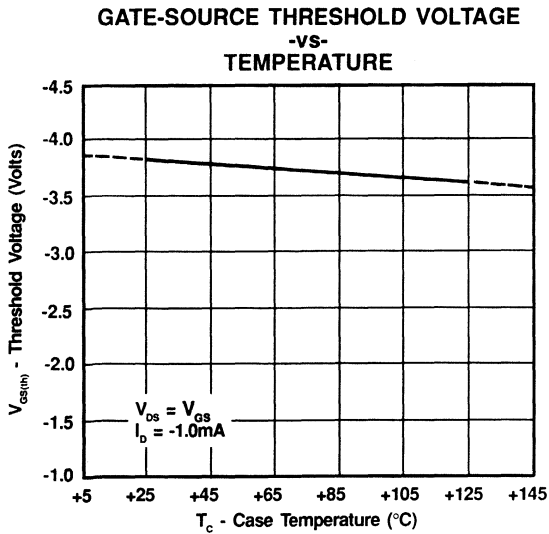
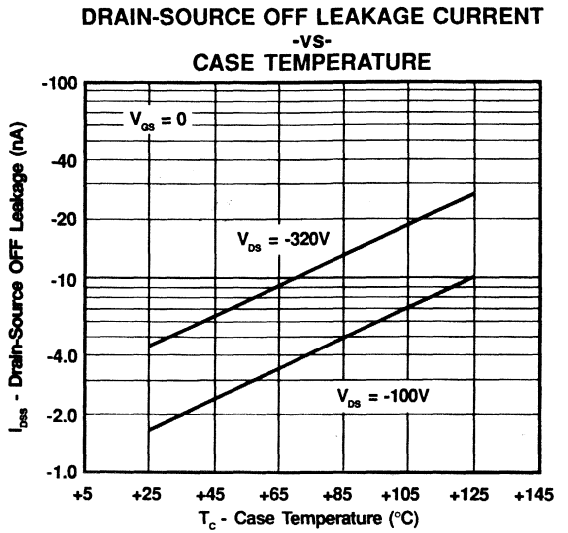
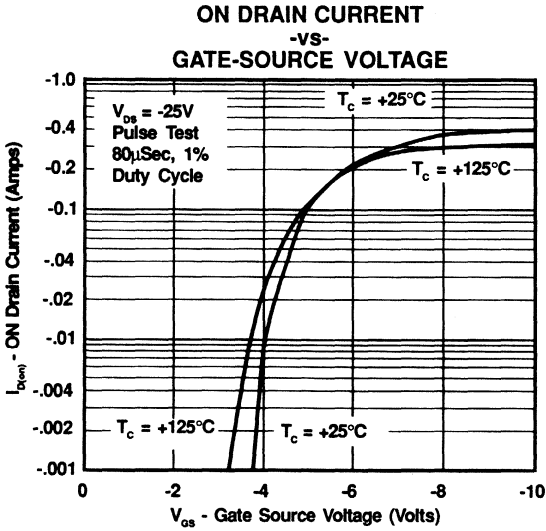
ON RESISTANCE -vs- GATE-SOURCE VOLTAGE



ON RESISTANCE -vs- GATE-SOURCE VOLTAGE



TYPICAL PERFORMANCE CHARACTERISTICS ($T_c = +25^\circ\text{C}$ unless otherwise noted)



P-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION



FEATURES

- Gate Stand-off Voltage, $\pm 40V$ min.
- Low Output and Transfer Capacitances
- N-Channel Complements Available

APPLICATIONS

- Motor Controls
- Logic Interfaces
- Pulse Amplifiers

ABSOLUTE MAXIMUM RATINGS ($T_c = +25^\circ C$ unless otherwise noted)

Drain-Source Voltage		
VP1008	-100V
VP0808	-80V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)		
VP1008	-100V
VP0808	-80V
Gate-Source Voltage		
.....	$\pm 40V$
Continuous Drain Current		
	$T_c = +100^\circ C$	$T_c = +25^\circ C$
TO-92 Pkg.	-13A
TO-237 Pkg.	-21A
		-33A
Peak Pulsed Drain Current		
.....	-3.0A

Maximum Power Dissipation

	$T_c = +100^\circ C$	$T_c = +25^\circ C$
TO-92 Pkg.	0.4W
TO-237 Pkg.	3.0W
		0.6W
		4.3W

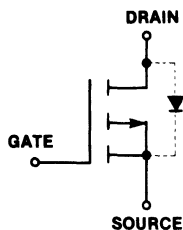
Linear Derating Factor

	Junction to Ambient	Junction to Case
	($mW/^\circ C$)	($mW/^\circ C$)
TO-92 Pkg.	5.33
TO-237 Pkg.	8.0
		24
		34

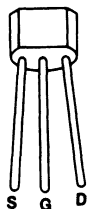
Operating Junction and Storage

Temperature Range	-55 to +150 $^\circ C$
Lead Temperature (1/16" from mounting surface for 10 Sec)	+300 $^\circ C$

PIN CONFIGURATIONS

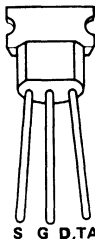


TO-226AA
(TO-92)



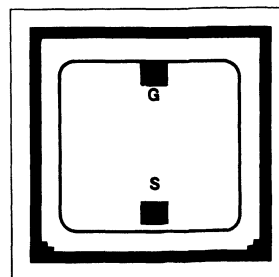
See Package 5

TO-237



See Package 7

CHIP CONFIGURATION



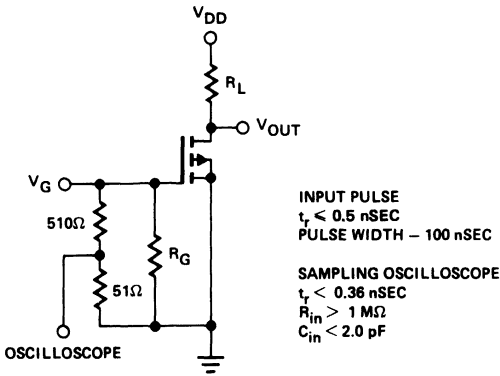
Dimensions: .054 x .051 x .020 in.
Drain is backside contact.

ELECTRICAL CHARACTERISTICS (T_c = +25°C unless otherwise noted)

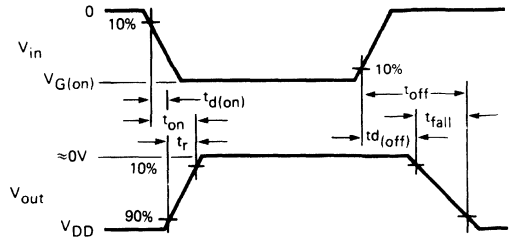
#	CHARACTERISTIC	VP0808			VP1008			UNIT	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
1	BV _{DSS} Drain-Source Breakdown Voltage	-80			-100			V	I _D = -10μA, V _{GS} = 0
2	V _{GS(th)} Gate-Source Threshold Voltage	-2.0		-4.5	-2.0		-4.5	V	V _{DS} = V _{GS} I _D = -1.0mA
3	I _{GAS} Gate-Body Leakage Current			-100			-100	nA	V _{GS} = -30V, V _{DS} = 0
4				100			100		V _{GS} = +30V, V _{DS} = 0
5	I _{DSS} Drain-Source OFF Leakage Current			-10				μA	V _{DS} = -80V
6				-500					V _{GS} = 0
7							-10		V _{DS} = -100V
8							-500		V _{GS} = 0
9	I _{D(on)} ON Drain Current ⁽¹⁾	-1.1			-1.1			A	V _{DS} = -25V, V _{GS} = -10V
10	V _{DS(on)} Drain-Source ⁽¹⁾ ON Voltage		-4.5	-5.0		-4.5	-5.0	V	V _{GS} = -10V, I _D = -1.0A
11	r _{DS(on)} Drain-Source ⁽¹⁾ ON Resistance		4.5	5.0		4.5	5.0	ohms	V _{GS} = -10V
12				8.0			8.0		I _D = -1.0A
13	g _{fs} Common-Source ⁽¹⁾ Forward Transcond.	200	270		200	270		mS	V _{DS} = -25V, I _D = -0.5A, f = 1KHz
14	C _{iss} Common-Source Input Capacitance		60	150		60	150	pF	V _{DS} = -25V, V _{GS} = 0 f = 1MHz
15	C _{rrs} Common-Source Reverse Transfer Capacitance		8.0	25		8.0	25		
16	C _{oss} Common-Source Output Capacitance		11	60		11	60		
17	t _{d(on)} Turn-ON Delay Time			10			10	nsec	V _{DD} = -25V R _L = 45 ohms R _G = 25 ohms V _{G(on)} = -10V
18	t _r Rise Time			15			15		
19	t _{d(off)} Turn-OFF Delay Time			10			10		
20	t _f Fall Time			15			15		
21	I _S Continuous Source Current	-0.21			-0.21			A	TO-92 Pkg.
22			-0.33			-0.33			
23	I _{SM} Peak Source Current ⁽¹⁾			-3.0			-3.0		
24	V _{SD} Source-Drain ⁽¹⁾ Forward Voltage		1.2			1.2		V	V _{GS} = 0
25				1.2		1.2			I = .21A, TO-92 Pkg. I = .33A, TO-237 Pkg.

Note 1: Pulse Test 80μSec, 1% Duty Cycle

SWITCHING TIME TEST CIRCUIT

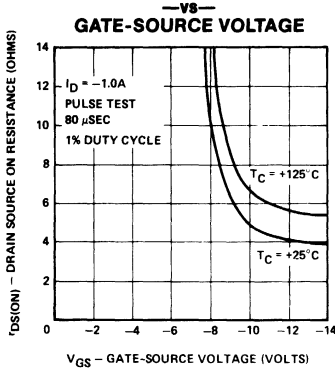


TEST WAVEFORMS

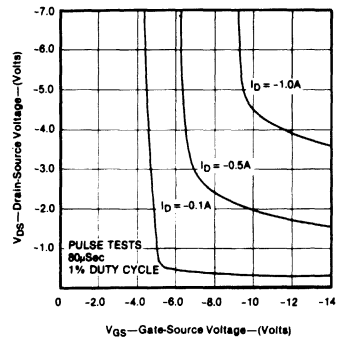


TYPICAL PERFORMANCE CHARACTERISTICS ($T_c = +25^\circ\text{C}$ unless otherwise specified)

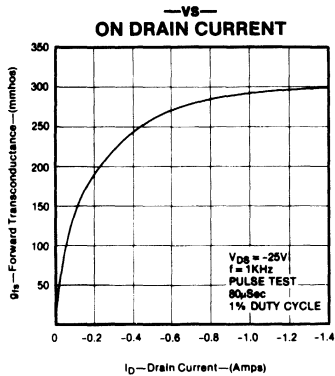
DRAIN-SOURCE ON RESISTANCE



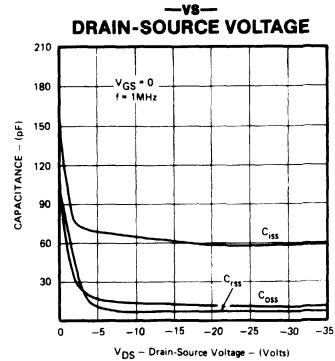
ON VOLTAGE CHARACTERISTICS



FORWARD TRANSCONDUCTANCE



CAPACITANCES



N-CHANNEL ENHANCEMENT-MODE QUAD D-MOS POWER FET ARRAY

ORDERING INFORMATION



FEATURES

- Inherent Current Sharing Capability when Paralleled
- Simple Straightforward DC Biasing
- Extended Safe Operating Area
- CMOS and TTL Compatible

APPLICATIONS

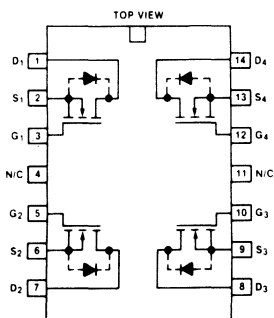
- High-Speed Pulse Amplifiers
- CMOS Logic to High-Current Interfaces
- High-Speed Switching
- Line Drivers
- Stepper Motor Drivers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise specified)

Drain-Source Voltage60V		
Drain-Gate Voltage (V _{GS} = 0)60V		
Gate-Source Voltage±40V		
Continuous Drain Current			
	T _A = 25°C	T _C = 25°C	
Total Package	.29	.51	A
Single Device	.20	.36	A
Peak Pulsed Drain Current1.0A		
Continuous Device Dissipation			
	T _A = +25°C	T _C = +25°C	
Total Package	.64	2.0	W
Single Device	.30	1.0	W

Linear Derating Factor			
	T _A = +25°C	T _C = +25°C	
Total Package	5.1	16	mW/°C
Single Device	2.4	8.0	mW/°C
Operating Junction			
Temperature Range-55 to +150°C		
Storage Temperature Range-55 to +150°C		
Lead Temperature (1/16" from mounting surface for 30 Sec)+260°C		

SCHEMATIC DIAGRAM



PACKAGE DIMENSIONS

14 PIN PLASTIC DIP

(See Package 9)

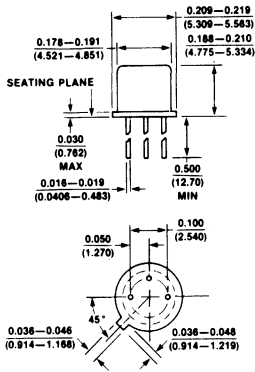
ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

#	CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS
1	STATIC	BV_{DSS} Drain-Source Breakdown Voltage	60	105		V	$I_D = 100\mu\text{A}, V_{GS} = 0$
2		$V_{GS(th)}$ Gate Source Threshold Voltage	0.8	1.9	2.5	V	$V_{DS} = V_{GS}, I_D = 1.0\text{mA}$
3		I_{GBS} Gate-Body Leakage Current		.10	100	nA	$V_{GS} = 10\text{V}$
4				10	500		$V_{DS} = 0$
5				-.10	-100		$V_{GS} = -10\text{V}, V_{DS} = 0$
6		I_{DSS} Drain-Source OFF Leakage Current		.10	10	μA	$V_{DS} = 60\text{V}$
7				10	500		$V_{GS} = 0$
8		$I_{D(on)}$ Drain-Source ON Current (Note 1)		0.2	1.3	A	$V_{GS} = 5\text{V}$
9				0.5	2.5		$V_{DS} = 10\text{V}$
10							$V_{GS} = 10\text{V}$
11		$V_{DS(on)}$ Drain-Source ON Voltage (Note 1)			1.50	V	$V_{GS} = 5\text{V}, I_D = 0.2\text{A}$
12					1.65		$V_{GS} = 10\text{V}, I_D = 0.3\text{A}$
13					7.5		$V_{GS} = 5\text{V}, I_D = 0.2\text{A}$
14					5.5		$V_{GS} = 10\text{V}, I_D = 0.3\text{A}$
15	DYNAMIC	g_{fs} Common-Source Forward Transcond (Note 1)	100	400		mmhos	$V_{DS} = 10\text{V}, I_D = 0.5\text{A}$ $f = 1\text{KHz}$
16		C_{iss} Common-Source Input Capacitance			60	pF	$V_{DS} = 25\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$
17		C_{rss} Common-Source Reverse Transfer Capacitance			5.0		
18		C_{oss} Common-Source Output Capacitance			25		
19		t_{on} Turn-ON Time			10		
20		t_{off} Turn-OFF Time			10		

Note 1: Pulse Test 80 μSec , 1% Duty Cycle

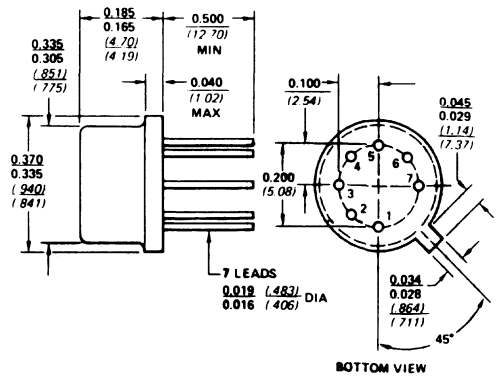
SECTION 4

Package 1 (TO-18) TO-206AA



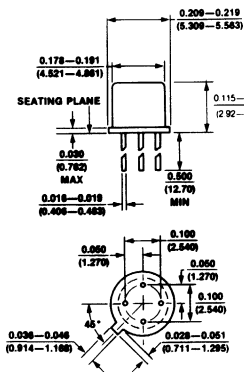
All Dimensions in inches and (millimeters)

Package 4 (TO-78)



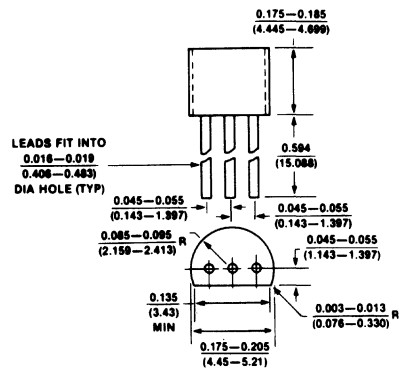
All Dimensions in inches and (millimeters)

Package 2 (TO-52) 4-Lead



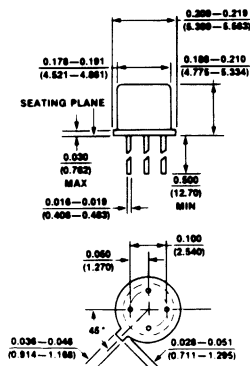
All Dimensions in inches and (millimeters)

Package 5 (TO-92) TO-226AA



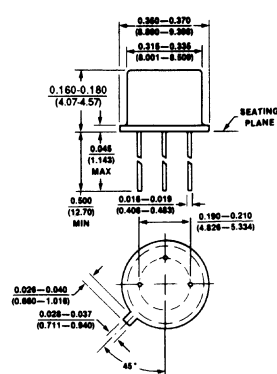
All Dimensions in inches and (millimeters)

Package 3 (TO-72) TO-206AF



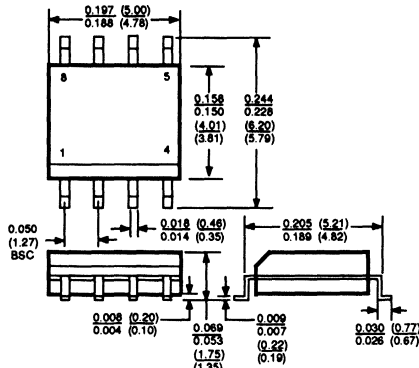
All Dimensions in inches and (millimeters)

Package 6 (TO-39) TO-205AF



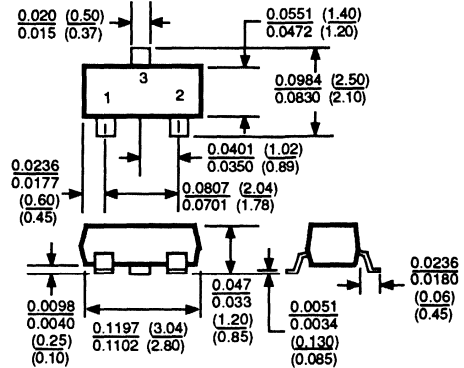
All Dimensions in inches and (millimeters)

Package 19 (SO-8)



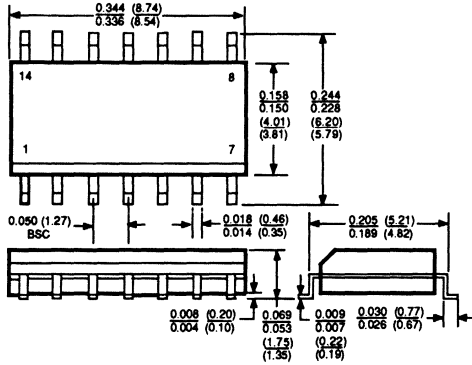
All Dimensions in Inches and (millimeters)

Package 22 (SOT-23) TO-236AA



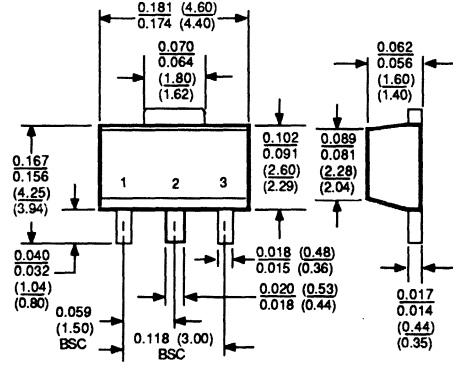
All Dimensions in Inches and (millimeters)

Package 20 (SO-14)



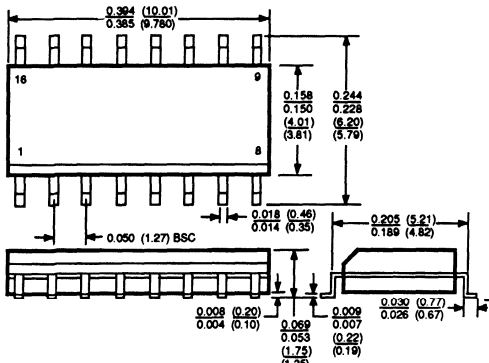
All Dimensions in Inches and (millimeters)

Package 23 (SOT-89) TO-243AA



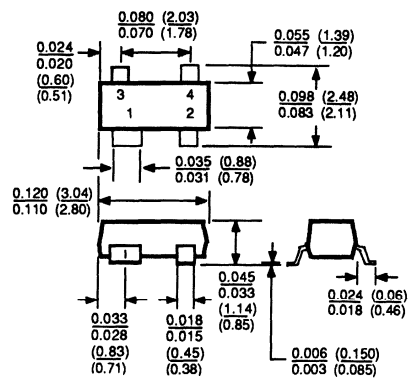
All Dimensions in Inches and (millimeters)

Package 21 (SO-16)



All Dimensions in Inches and (millimeters)

Package 24 (SOT-143)



All Dimensions in Inches and (millimeters)

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SECTION 5

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AN02	CDG4469J APPLICATIONS NOTE A total of 4 gain control circuits are described for the CDG4469J 8-Bit Digital Controlled Attenuator. In addition, a distortion compensation circuit is described and five performance curves for harmonic distortion, phase shift and attenuation change with temperatures are provided.	5-5, 5-6, 5-7
AN03	SPICE PARAMETERS A SD215DE, N-Channel, Depletion-Mode, Lateral D-MOS FET is used as an example for DC, AC and TRANSIENT Analysis.	5-8, 5-9, 5-10, 5-11
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DESIGN CONSIDERATIONS FOR ANALOG SWITCHES USING LATERAL D-MOS FETs

INTRODUCTION

Two Lateral D-MOS FET products recently introduced by Topaz Semiconductor, the SD211A and SD215A have maximum values of ON Resistance ($r_{DS(on)}$) specified in practical analog switch configurations. The SD211A, normally used as a +30V switch driver, also has applications as a $\pm 5V$ analog switch.

CONFIGURATION

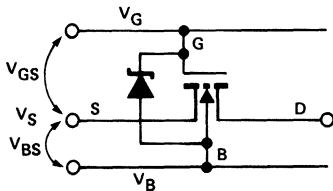


Figure 1

MAXIMUM VOLTAGES

DEVICE	VS(1) ANALOG INPUT VOLTAGE RANGE	VG(2) CONTROL INPUT VOLTAGE RANGE	VB(3) BODY VOLT.
SD211A	-5.0V to +5.0V	-10V to +15V	-10V
SD215A	-10V to +10V	-15V to +15V	-15V

- (1) Maximum range of Analog Input Voltage (V_s) is limited by the Source-Drain Breakdown Voltage (BV_{SD}) of the D-MOS FET. If the breakdown voltage is exceeded the analog switch will have high OFF Leakage.
- (2) Control Input Voltage (V_G) must be set so that it turns the D-MOS FET OFF with the Analog Input (V_s) at the most negative voltage and ON at the most positive Analog Input voltage.
- (3) As a minimum, Body Bias Voltage (V_B) is set to the most negative point in the circuit to prevent the Gate protective diode or internal device diodes being forward biased under any condition of applied voltages. In practice V_B should remain

negative with respect to V_s to avoid excessive increases in Source-to-Body Capacitance.

DESIGN CONSIDERATIONS

The ON Resistance ($r_{DS(on)}$) of the D-MOS FET depends upon the Gate-Source Voltage (V_{GS}) added to Threshold Voltage ($V_{GS(th)}$) of the FET. The lowest or least voltage added to Threshold Voltage or highest ON Resistance is when the analog input is at the most positive value. The following curve illustrates ON Resistance change as a function of Analog Input Voltage:

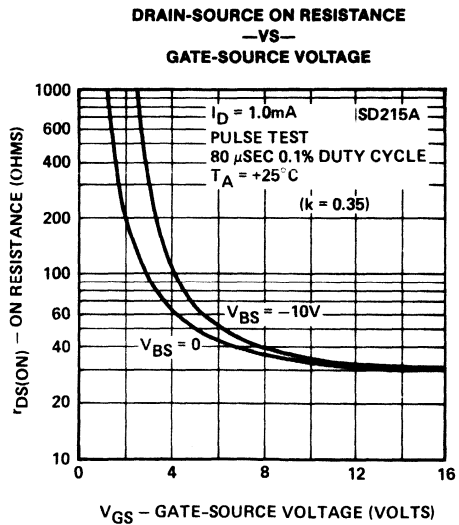


Figure 2

GAMMA EFFECT

The actual Threshold Voltage in an analog switch configuration is higher than the value on the data sheet because of the effect of Body-Source Voltage (V_{BS}). The following curve illustrates change in Threshold Voltage as a function of Body to Source Bias Voltage:

DESIGN CONSIDERATIONS FOR ANALOG SWITCHES USING LATERAL D-MOS FETs (continued)

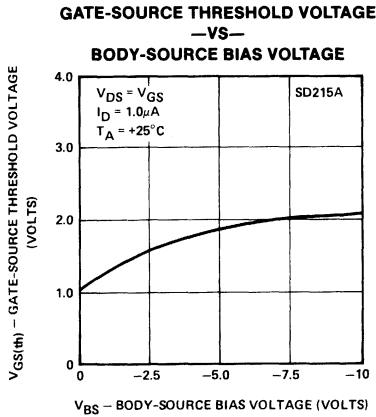


Figure 3

The change or increase in Threshold Voltage with Body to Source Bias Voltage applied is described by the following equation:

$$V_{GS(th)1} = V_{GS(th)0} + k \sqrt{|V_{BS}|}$$

The “k factor” or Gamma controls the increase in Threshold Voltage or “Up Threshold” with Body Voltage. $V_{GS(th)}$ also changes with temperature as shown on the following curve:

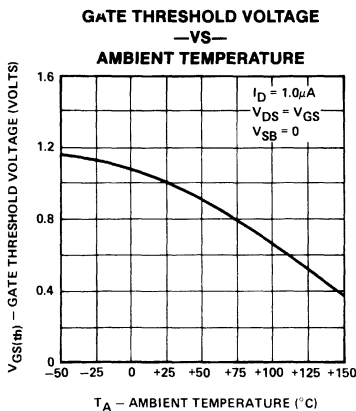


Figure 4

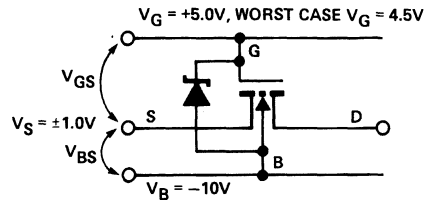
CONCLUSION

Low Gamma D-MOS FETs from Topaz Semiconductor offer design solutions for low Gate Drive Voltage Analog Switches.

DESIGN EXAMPLE:

Use an SD215A to switch a ± 1.0 Volt signal in a 5.0 Volt system. Compare test results to those obtained with a competitor’s SD215.

CONFIGURATION



$$V_{GS(on)} = +3.5V \text{ min.}, V_{BS} = -11V$$

$$V_{GS(th)1} = V_{GS(th)0} + k \sqrt{|V_{BS}|} \tag{1}$$

$$r_{DS(on)} = \frac{1}{K(V_{GS(on)} - V_{GS(th)1})} \tag{2}$$

Note: K is the Device Constant, $K \approx \frac{W\mu Co}{L}$ for this type of Lateral D-MOS, $K \approx .003$

TEST RESULTS

1. Topaz SD215A, (k = 0.35)

$V_{GS(th)0}$	$V_{GS(th)1}$	$r_{DS(on)}$
0.75V	1.91V	209 ohms
1.00V	2.16V	248 ohms
1.25V	2.41V	305 ohms
1.50V	2.66V	396 ohms

2. Competitor’s SD215, (k = 0.65)

$V_{GS(th)0}$	$V_{GS(th)1}$	$r_{DS(on)}$
0.75V	2.90V	555 ohms
1.00V	3.15V	952 ohms
1.25V	3.40V	3300 ohms
1.50V	3.65V	OFF

DESIGN CONSIDERATIONS FOR THE CDG4469J DIGITAL CONTROLLED ATTENUATOR

INTRODUCTION

Conventional methods of controlling amplifier gain such as change of device transconductance or by resistor divider networks can result in unwanted phase shift or loss of bandwidth.

Typical low frequency gain control circuits involve changing gain setting resistors which causes changes in offset and, when compensated, adds unwanted phase shift. To minimize both effects the gain setting resistors will have to be of low value.

In high frequency applications a lot of extra circuitry is required to compensate and stabilize circuits. Here gain control is done mostly by varying the transconductance of individual gain stages. The result is a change from the optimum operating point to one that is less desirable. The side effects are an increase in noise, loss of bandwidth, shift in input and output impedance and unwanted phase shift. In narrow band amplifiers this causes mismatch to filters and the degradation of in-band frequency components.

The CDG4469J Digital Controlled Attenuator meets the need for an attenuation concept that overcomes these problems and provides gain control over a wide dynamic range. The CDG4469 allows gain control over a range of 127.5dB in 0.5dB steps via an 8-bit digital parallel control port over a wide frequency range with constant input and output impedance. Since the CDG4469 input and output ports are strictly resistive, the device can be placed directly in a DC path. This capability is very useful when controlling the gain of an amplifier by the feedback loop.

GAIN CONTROL CIRCUITS

Figure 1 shows a circuit for the CDG4469J used in a high frequency gain control application.

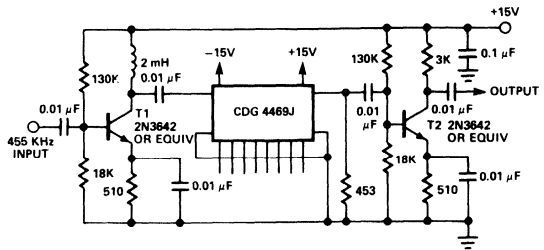


Figure 1

The circuit uses an NPN transistor biased at the optimum operating point with an RF choke as the DC pass for the collector. The CDG4469 is AC coupled to the collector of T1 and becomes the effective load of that gain stage. The output of the CDG4469 is then coupled to the input of the next gain stage, T2 and sees an AC load of 453 ohms. Gain can then be digital controlled with no effect on the transfer characteristic.

An amplifier gain control circuit which includes a band pass filter, where matching is critical, is shown in figure 2:

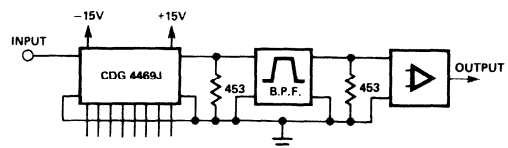


Figure 2

In this circuit the CDG4469 Attenuator can be placed either in front or after the filter. A change in gain of the Attenuator will have no effect on the band-pass characteristic because input and output impedances of the attenuator are constant. Since the CDG4469 can handle large signals and has the noise voltage characteristic of a 600 ohm resistor, it can be placed in the circuit directly in front of the amplifier.

DESIGN CONSIDERATIONS FOR THE CDG4469J DIGITAL CONTROLLED ATTENUATOR (continued)

A circuit which controls gain by controlling the amount of feedback is shown in Figure 3:

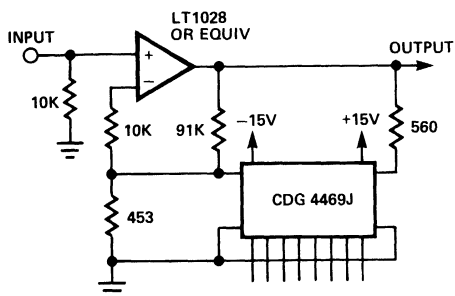


Figure 3

In the above circuit the CDG4469 is an excellent choice because of wide bandwidth, low phase shift and constant input and output impedance. Placing a resistor across the attenuator limits the maximum gain and leaves the amplifier in a controlled operating range.

Should there be a need for attenuation only, the CDG4469 can be placed directly in the signal path of an amplifier as shown in Figure 4:

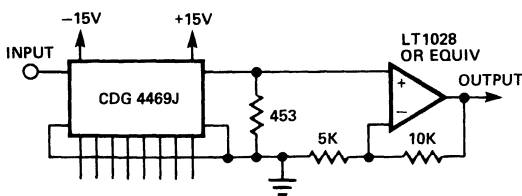


Figure 4

As indicated above, the added noise voltage from the CDG4469 is equal to that of a 600 ohm resistor and is constant over the entire attenuation control range.

DISTORTION COMPENSATION CIRCUIT

An attenuator/amplifier circuit which uses power supply modulation to minimize total harmonic distortion is shown in Figure 5:

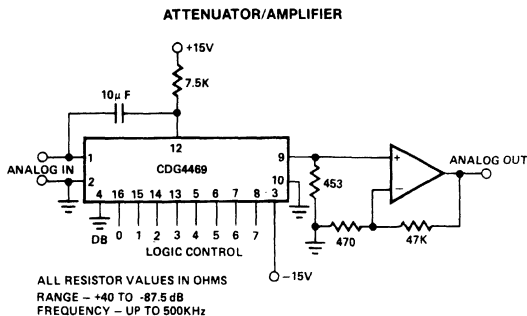


Figure 5

In the above circuit a portion of the analog input is added to the positive supply voltage because the 7.5K ohm resistor in series with the supply and the 650 ohm input resistor form a voltage divider network. This modulates the ON resistance of the internal FET switches to maintain constant insertion loss over the analog voltage input range. The 10µF capacitor used gives a low frequency corner of about 20 Hz.

ATTENUATOR CHARACTERIZATION

Figures 6, 7 and 8 show total harmonic distortion characteristics as a function of attenuation setting and level of analog input. The compensation circuit is the same as illustrated in Figure 5 above.

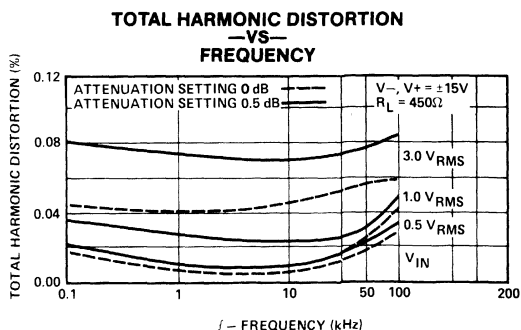


Figure 6

**DESIGN CONSIDERATIONS FOR THE
CDG4469J DIGITAL CONTROLLED ATTENUATOR
(continued)**

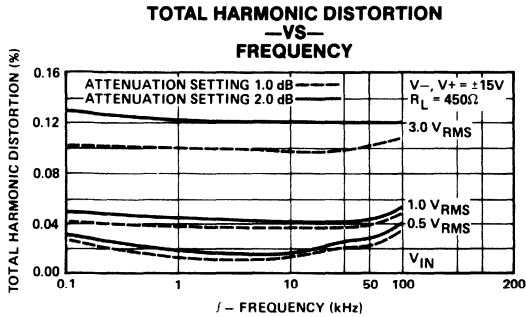


Figure 7

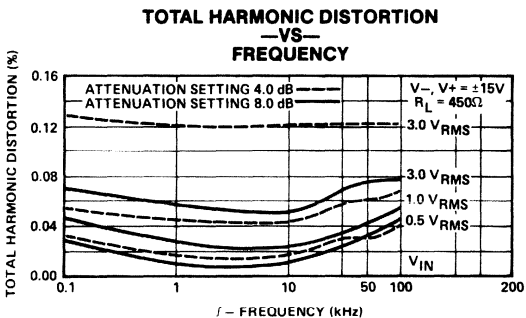


Figure 8

Figure 9 shows attenuation change -vs- attenuation setting -vs- ambient temperature. All attenuation changes are referenced to 0dB at an ambient temperature of +25°C.

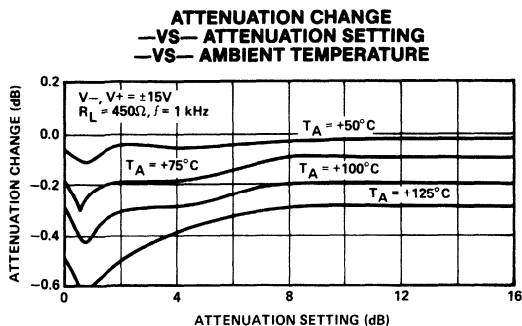


Figure 9

Figure 10 shows phase shift characteristics as a function of attenuation setting and logarithmic change in frequency.

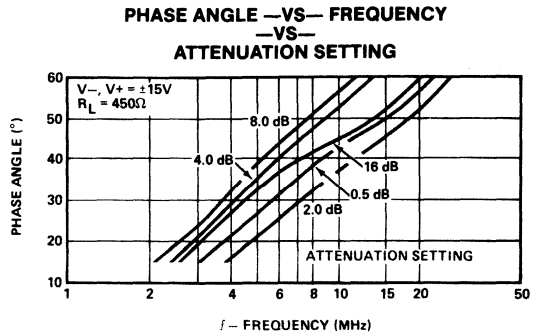


Figure 10

OTHER DESIGN CONSIDERATIONS

Analog input ground (pin 2) and analog output ground (pin 10) must be connected to a common point. Logic control ground (pin 4) is separate from analog ground.

The CDG4469 can be placed at the optimum point in any circuit and be controlled by a digital line. With latches added in front of the control inputs the CDG4469 attenuation settings can be retained until it is necessary to update them. This concept is very useful when the CDG4469 is controlled by a computer.

If attenuation steps of less than 0.5dB are required two CDG4469's can be connected in parallel. With two attenuators in parallel attenuation is 0.25dB per step and the total attenuation range is 63.75dB.

CONCLUSION

The CDG4469 attenuator with constant input and output impedance regardless of attenuation setting is adding new dimensions to the design of gain controlled amplifiers. The CDG4469 attenuation accuracy is maintained up to about 500KHz with full attenuation range and up to 5.0MHz with 6 bits or 31.5dB of attenuation range.

SPICE PARAMETERS AND MODELS N-CANNEL, DEPLETION-MODE LATERAL D-MOS FETs

INTRODUCTION

The popularity of SPICE simulation programs run on PCs has resulted in requests for SPICE Models of Topaz Semiconductor's devices. With the help of IS-Spice⁽¹⁾ and INTUSCOPE⁽¹⁾ programs, a DC model was generated for the SD215DE, an N-Channel, enhancement-mode, small signal, Lateral D-MOS Field Effect Transistor. Using design and process calculations and package measurements, additional SPICE parameters were obtained to complete the AC and Transient models. A complete listing of SPICE 2 Model Parameters is included at Appendix A.

The following types of analysis can be run on Lateral D-MOS FETs using the INTUSOFT programs.

1. DC Analysis
 - a. Operating Point
 - b. Transfer Function sensitivity
 - c. Curve families
2. AC Analysis
 - a. Transfer Function
 - b. Frequency Response
 - c. Distortion
 - d. Noise
3. Transient Analysis
 - a. Switching
 - b. Non-linear time domain
 - c. Fourier

DC ANALYSIS

The DC Model equations for the example are as follows;

Linear Region ($V_{GS} > V_{TH}$ and $V_{DS} < V_{GS} - V_{TH}$)

$$I_{DS} = \frac{KPW}{L} (V_{GS} - V_{TH} - V_{DS}/2) V_{DS} (1 + LAMBDA \cdot V_{DS})$$

Saturation Region ($V_{GS} > V_{TH}$ and $V_{DS} > V_{GS} - V_{TH}$)

$$I_{DS} = \frac{KPW}{2L} (V_{GS} - V_{TH})^2 (1 + LAMBDA \cdot V_{DS})$$

$$V_{TH} = V_{TO} + GAMMA \cdot (\sqrt{PHI} - \sqrt{V_{BS}} - \sqrt{PHI})$$

$$KP' = KP \left[\left(\frac{\epsilon_S}{\epsilon_{OX}} \right) \left(\frac{UCRIT \cdot T_{OX}}{V_{GS} - V_{TH} - UTRA \cdot V_{DS}} \right) \right]$$

$$KP = UO \cdot C_{OX}$$

$$C_{OX} = \frac{\epsilon_{OX}}{T_{OX}}$$

1. IS-Spice and INTUSCOPE are copyrighted trade names of Intusoft, San Pedro, CA 90734-6607

$\epsilon_S = 10.36 \times 10^{13}$ F/CM (Silicon permittivity)
 $\epsilon_{OX} = 3.45 \times 10^{13}$ F/CM (Silicon Dioxide permittivity)

The SD215 DC Model is illustrated in Figure 1;

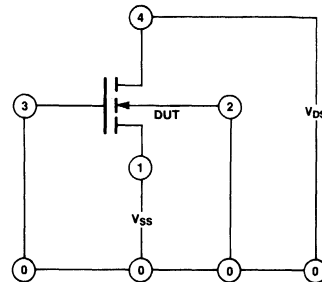


Figure 1. DUT and Model Nodes

The SD215 SPICE 2 Model Parameters are listed below;

	SD215DC
TYPE	NMOS
LEVEL	2.000
VTO	1.000
KP	1.14D-05
GAMMA	.600
PHI	.760
LAMBDA	1.00D-02
TOX	1.00D-07
TPG	.000
UO	330.000
UCRIT	1.00D+04
UEXP	.240
UTRA	.500

The Input Listing for DC Analysis is as follows;

```
*SD215DC
M1 4 3 1 2 SD215DC L=1.4E-6 W=9.1E-4
AD=2.4E-8 AS=3E-8 PD=9.1E-4 PS=9.1E-4 OFF
VGS 3 0 DC 10
VDS 4 0 DC 10
VBS 0 2 DC 0
VSS 1 0 DC 0
.MODEL SD215DC NMOS LEVEL=2
+ LAMBDA=1E-2 PHI=0.76 GAMMA=0.6
+ VTO=1.0 TOX=1E-7 TPG=0
+ UO=330 UCRIT=1E4 UEXP=0.24 UTRA=0.5
.DC VDS 0 10 0.5 VGS 0 10 1
.OPTIONS LIMPTS=500
.PRINT DC V(4) I(VSS)
.END
```

DC ANALYSIS (Continued)

Calculated and measured values for 'Family Characteristics' are illustrated in Figure 2;

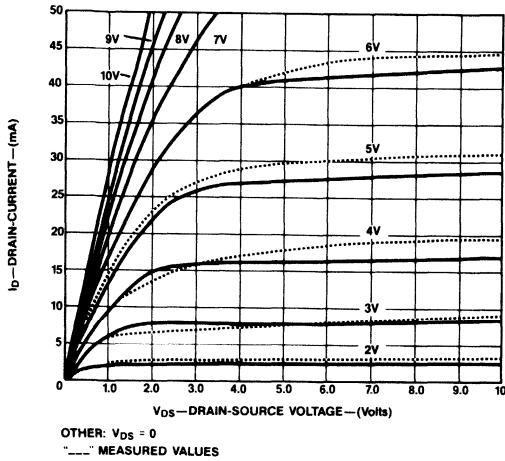


Figure 2: SD215 Family Characteristics

AC ANALYSIS

The SD215 chip in a TO-72 package is denoted as SD215DE. The AC Model is shown in Figure 3;

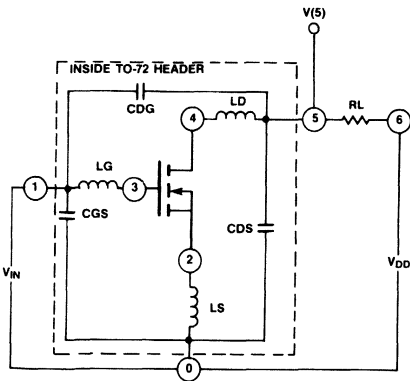


Figure 3: AC Model

The SD215DE SPICE 2 Model Parameters are listed below;

	SD215AC
TYPE	NMOS
LEVEL	2.000
VTO	1.000
KP	1.14D-05
GAMMA	.600
PHI	.760
LAMBDA	1.00D-02
CBD	2.80D-12
CBS	1.60D-11
IS	1.00D-15
PB	.050
CGSO	4.60D-10
CGDO	7.70D-11
CGBO	3.00D-09
JS	2.88D-07
TOX	1.00D-07
NFS	8.10D+10
TPG	.000
UO	330.000
UCRIT	1.00D+04
UEXP	.240
UTRA	.500
NEFF	5.010

The Input Listing for AC calculations is as follows;

```
VIN 1 0 DC 5 AC 1
VDD 6 0 DC 20
RL 6 5 5700HMS
LG 1 3 4NH
LS 2 0 2NH
LD 5 4 4NH
CGS 1 0 0.31PF
CDS 5 0 0.34PF
CGD 1 5 0.03PF
M1 4 3 2 2 SD215AC L=1.4E-6 W=9.1E-4
AD=2.4E-8 AS=3E-8 PD=9.1E-4 PS=9.1E-4
.MODEL SD215AC NMOS LEVEL=2
+ LAMBDA=1E-2 PHI=0.76 GAMMA=0.6
+ VTO=1.0 TOX=1E-7 TPG=0
+ IS=1E-15 PB=0.05 JS=2.88E-7
+ NFS=8.1E10 NEFF=5.01
+ UO=330 UCRIT=1E4 UEXP=0.24 UTRA=0.5
+ CGSO=4.6E-10 CGDO=7.7E-11 CGBO=3E-9
+ CBD=2.8E-12 CBS=1.6E-11
.AC DEC 50 1MEGHZ 1GHZ
.PRINT AC V(5) V(1) I(VDD)
.END
```

AC ANALYSIS (Continued)

A frequency response curve using calculated values is shown in Figure 4;

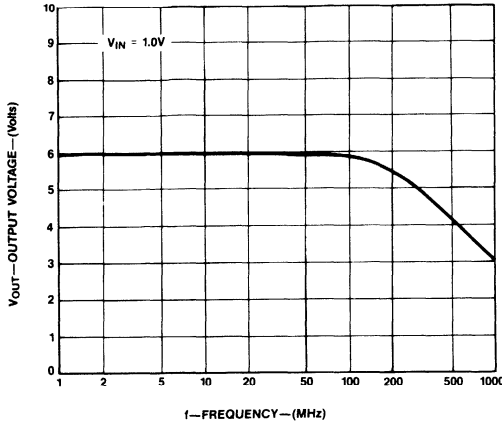


Figure 4: Voltage Gain vs. Frequency

TRANSIENT ANALYSIS

The SD215 DE Switching Model is shown in Figure 5;

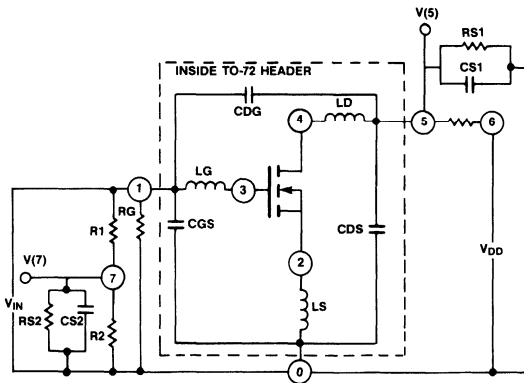


Figure 5: Switching Model

The SD215DE SPICE 2 Model Parameters for switching are identical to AC ANALYSIS Parameters listed above.

The input listing for switching time calculations is as follows;

```
R1 1 7 510OHMS
R2 7 0 510OHMS
RS1 7 0 1MEGOHMS
CS1 7 0 2PF
RS2 5 0 1MEGOHMS
CS2 5 0 2PF
RL 6 5 680OHMS
RG 1 0 510OHMS
CGS 1 0 0.31PF
CDS 5 0 0.34PF
CDG 1 5 0.03PF
LG 1 3 4NH
LS 2 0 2NH
LD 5 4 4NH
M1 4 3 2 2 SD215SW L=1.4E-6 W=9.1E-4 AD=2.4E-8
AS=3E-8 PD=9.1E-4 PS=9.1E-4
VIN 1 0 AC 1 PULSE 0 10 0 1NS 1NS 3NS 20NS
VDD 6 0 DC 5
.MODEL SD215SW NMOS LEVEL=2
+ LAMBDA=1E-2 PHI=0.76 GAMMA=0.6
+ VTO=1.0 TOX=1E-7 TPG=0
+ NFS=8.1E-10 NEFF=5.01
+ UO=330 UCRIT=1E4 UEXP=0.24 UTRA=0.5
+ IS=1E-15 PB=0.05 JS=2.88E-7
+ CGSO=4.6E-10 CGDO=7.7E-11 CGBO=3E-9
+ CBD=2.8E-12 CBS=1.6E-11
.TRAN 1NS 20NS
.PRINT TRAN V(5) V(7)
.END
```

Turn ON and Turn OFF delay are not included in results. Calculated values for Rise and Fall Times are shown in Figure 6;

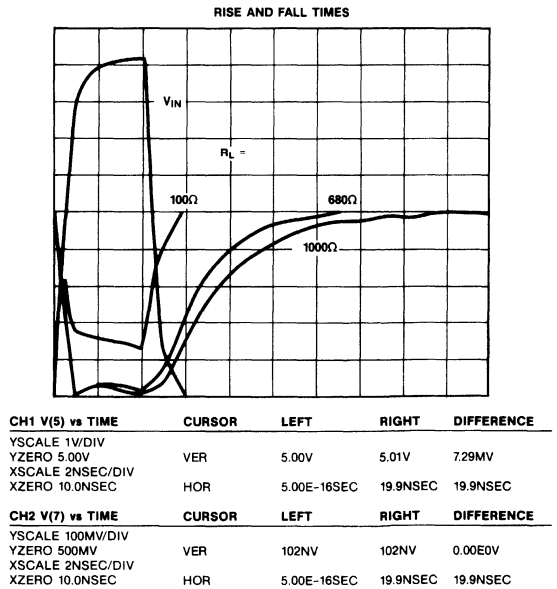


Figure 6. Rise and Fall Times

CONCLUSION

SPICE 2 Model Parameters when combined with accurate circuit models are a very useful tool for evaluating the performance of D-MOS FETs in switching and amplifier configurations. The examples illustrated above form only a very small portion of the work completed to date. Contact Topaz Semiconductor direct for additional data on the SD215 and other D-MOS FET products.

In addition to the SD215, Topaz manufactures many other high performance Lateral and Vertical Technology D-MOS Field Effect Transistors and CMOS/D-MOS Integrated Circuits. CMOS/D-MOS ICs are offered as end products such as Analog Switches and Multiplexers or contained in Digital Controlled Attenuator hybrid products. For additional product information on discrete products and ICs refer to product selector guides contained in the current Data Book. A summary listing of the types of discrete D-MOS FETs offered by Topaz is given below;

1. Small-Signal, Enhancement-Mode, N-Channel Lateral D-MOS. 10-30V and 50-70 ohms.
2. Small-Signal, Depletion Mode, N-Channel Lateral D-MOS. 10-20V and 75-150 ohms.
3. Medium-Power, Enhancement-Mode, N-Channel Lateral D-MOS. 20-25V and 4-8 ohms.
4. Medium-Power and High-Voltage, Enhancement Mode, N-Channel Lateral D-MOS. 60-100V and 9-10 ohms.
5. Small-Signal and Medium Power, Enhancement Mode, N-Channel, Vertical D-MOS. 40-800V and 0.4-700 ohms.
6. Small-Signal and Medium Power, Enhancement Mode, P-Channel, Vertical D-MOS. -40V to -400V and 5 ohms to 700 ohms.

APPENDIX A

SD215 SPICE 2 Model Parameters

Spice Keyword	Value	Units
L	1.4E-6	M
W	9.1E-4	M
AD	2.4E-8	M ²
AS	3E-8	M ²
PD	9.1E-4	M
PS	9.1E-4	M
VTO	1.0	V
LAMBDA	1.5E-2	V ⁻¹
GAMMA	0.6	V ^{1/2}
PHI	0.76	V
TPG	0	—
TOX	1E-7	M
NFS	8.1E-10	em ⁻²
NEFF	5.01	—
PB	0.05	V
IS	1E-15	A
JS	2.88E-7	A/M ²
UO	330	CM ² /V-S
UCRIT	1E4	V/cm
UTRA	0.5	—
UEXP	0.24	—
CBD	2.8E-12	F
CBS	1.6E-11	F
CGDO	7.7E-11	F/M
CGSO	4.6E-10	F/M
CGBO	3E-9	F/M

LATERAL D-MOS FIELD EFFECT TRANSISTORS CHARACTERISTICS

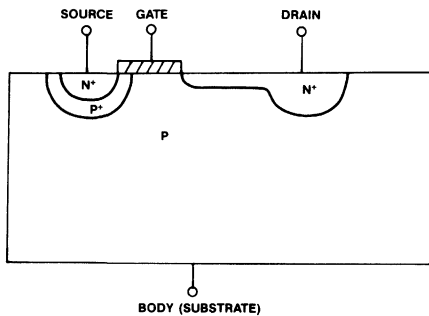
INTRODUCTION

D-MOS is an acronym for "double diffused metal oxide semiconductor". Originally introduced in the early 1970's the technology has evolved into two distinct product types, Lateral and Vertical D-MOS. This application note discusses the three types of Lateral D-MOS available from Topaz Semiconductor.

CROSS-SECTIONAL DIAGRAMS

(1) N-Channel, Enhancement and Depletion Mode structure.

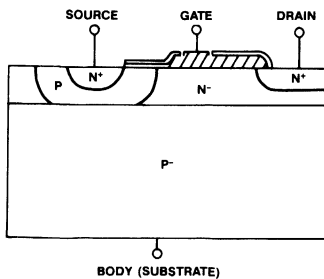
Figure 1.



Note: Enhancement and Depletion mode types have identical cross-sections. The mode of the device is set by Threshold Shift Implant.

(2) N-Channel, Enhancement Mode, RESURF structure

Figure 2.



BIAS CONFIGURATIONS

(1) Enhancement Mode

Figure 3.

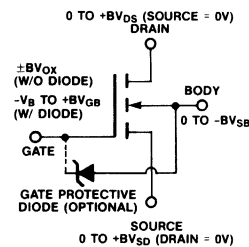
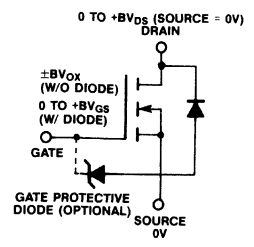


Figure 4.

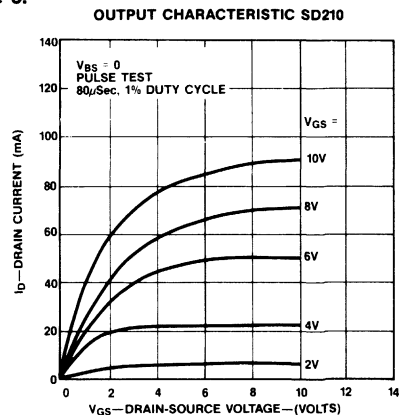


Four-terminal

Three-terminal

An example of 'Family Characteristics' applicable to three and four terminal Enhancement-Mode devices is shown in Figure 5;

Figure 5.

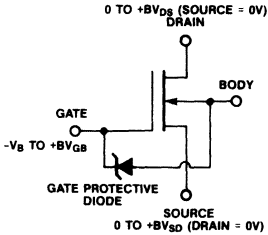


A three-terminal device, because the Body (Substrate) pin is connected to the Source, has a parasitic diode between the Drain and Source in the same way as a Vertical technology D-MOS FET. Four-terminal Lateral D-MOS has an advantage over Vertical D-MOS for ultra-high-speed and up to $\pm 10V$

analog switch applications because a switching circuit can be implemented with a single device with low capacitance. Lateral D-MOS devices with RESURF layers were introduced to fill the need for high speed switch drivers capable of operating at up to +100 volts. Epitaxial Lateral devices as a trade-off have low Source-Drain Break-down voltages (BV_{SDX}) and as such are not appropriate for four-terminal analog switch applications but have the ultra high speed characteristics of Lateral D-MOS.

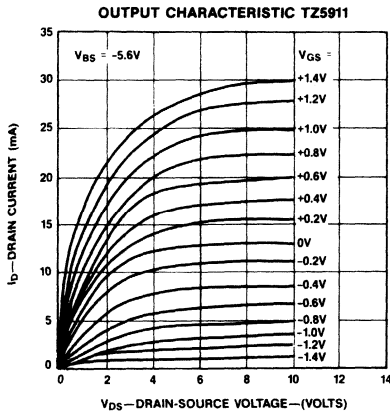
(2) Depletion Mode

Figure 6.



An example of 'Family Characteristics' for Depletion Mode devices is shown in Figure 7;

Figure 7.



In analog circuits Depletion-Mode (normally-on) Lateral D-MOS devices when compared to Enhancement Mode (normally-off) devices can offer advantages by choice of optimum operating point. Gate voltages positive with respect to the Source can be used to increase the dynamic range.

IMPORTANT DEVICE CHARACTERISTICS

(1) Body Bias Effect

Also called Gamma or Up-Threshold Voltage, this effect is present in all Lateral D-MOS FETs and is an important concern in any 4-terminal circuit such as a low Gate drive voltage analog switch. Body Bias Effect, which is defined as the change (increase) in Gate Threshold Voltage with Body to Source bias voltage applied, is described by the following equation;

$$V_{GS(th)1} = V_{GS(th)0} + k \sqrt{|V_{BS}|}$$

The lower the "k factor" or Gamma the better the performance in circuits such as low Gate Drive Voltage analog switches. The "k factor" is not a direct specified parameter but is included in test conditions for $r_{DS(on)}$ on data sheets for low Gamma devices such as the SD211A/SD215A.

The following curves show the effect of Gamma on Gate Threshold Voltage and Drain-Source ON Resistance.

Figure 8.

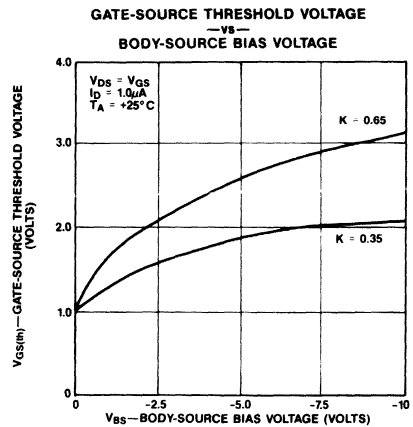
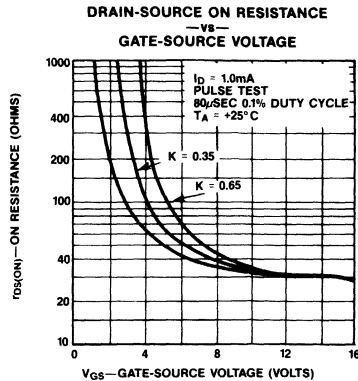


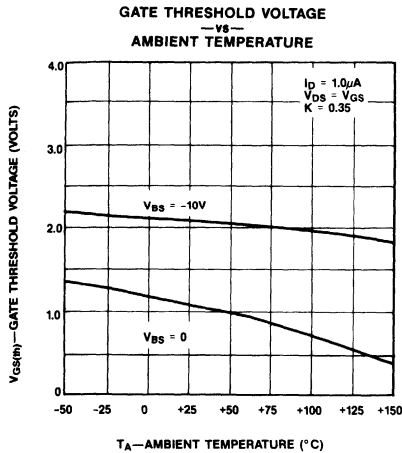
Figure 9.



(2) Gate-Source Threshold Voltage ($V_{GS(th)}$ or V_T)

Gate Threshold Voltage is temperature dependent. V_T change as a function of ambient temperature and Gamma is illustrated below.

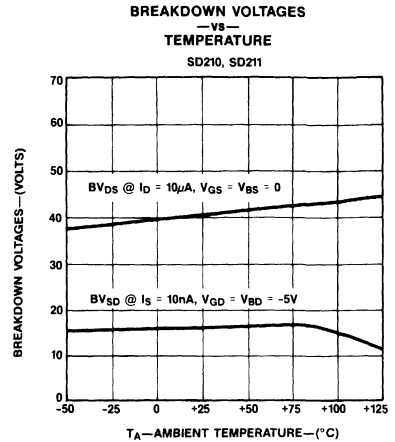
Figure 10.



(3) Breakdown Voltages vs Ambient Temperature

Source to Drain Breakdown Voltage (BV_{SD}) and Drain to Source Breakdown Voltage increase as temperature increases provided that leakages have not increased above test currents used to measure breakdown voltages. BV_{SD} and BV_{DS} also decrease as temperature decreases. Breakdown voltages as a function of ambient temperature are illustrated in Figure 11;

Figure 11.



(4) Leakage Currents vs Ambient Temperature

Source to Drain Leakage (I_{SD}) and Drain to Source Leakage (I_{DS}) increase as temperature increases. However, the leakage multiplication factor for an increase of 100°C (+25 to +125°C) can vary from 3X to 100X with typical increases about 10X. Another reason leakages do not multiply as much as expected is because some leakage seen at +25°C is due to package conductance. Typical values of I_{SD} and I_{DS} and how they vary with temperature are illustrated in Figure 12;

Gate to Body Leakage Currents (I_{GBS} or I_{GSS}) fall into two categories, leakage across non-diode protected Gates with no noticeable leakage multiplication with temperature and second leakage across Gate protected devices where leakage does multiply across the protective diode. A very important consideration in measuring leakage is to make sure that the Gate, which is ultra ESD sensitive even on devices with Gate protective diodes, is not damaged during the test. The best approach is to do a leakage test where voltage is applied and current is compared to a limit instead of a breakdown test where current is forced and voltage drop is compared to a limit. This is especially true on non-Gate protected devices. Leakage currents as a function of ambient temperature are illustrated in Figure 13;

Figure 12.

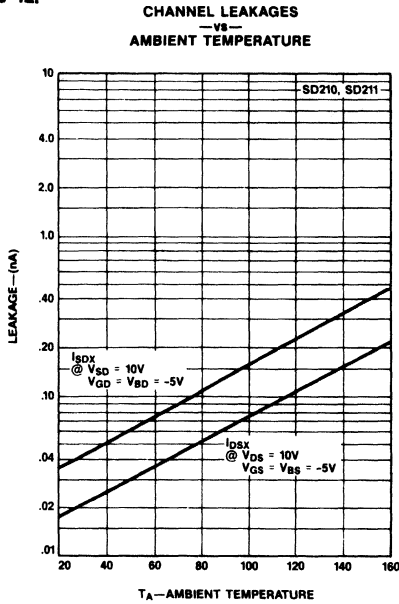
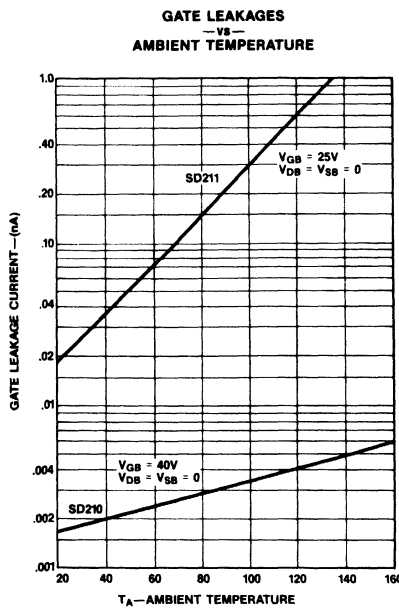


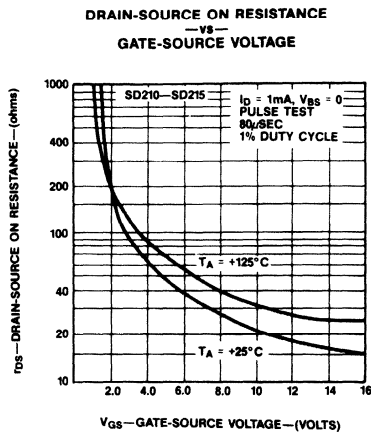
Figure 13.



(5) On Resistance vs Ambient Temperature

Drain to Source ON Resistance ($r_{DS(on)}$) increases as ambient temperature increases and decreases as ambient temperature decreases. For worst case design assume that $r_{DS(on)}$ increases +0.7% per degree Centigrade increase in temperature. In actual practice the TC is about +0.5% per degree Centigrade. Typical curves of On Resistance vs temperature for the SD210-SD215 series are shown in Figure 14.

Figure 14.



A COMMON GATE OSCILLATOR CIRCUIT UTILIZING THE TZ403BD

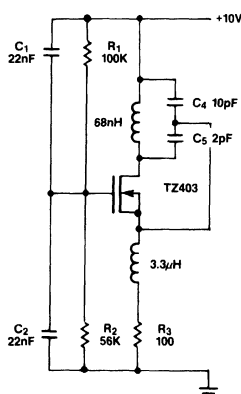
INTRODUCTION

The TZ403BD was selected for a single device Colpitts oscillator design because of low part cost while at the same time offering the high performance of Lateral D-MOS.

CIRCUIT DESCRIPTION

The circuit selected is illustrated in Figure 1;

Figure 1. 390MHz Oscillator



The single device Colpitts oscillator design shown above was selected because it should have very low even harmonics and no odd harmonics in the output while operating over a wide range. The tuned circuit is connected from the Drain of the TZ403 to the supply voltage with a capacitor divider which feeds into the Source of the TZ403 for oscillation. The Source resistor is selected to establish a stable operating point. The voltage across the resistor should be equal to the Gate Source voltage at the operating point. For the purest possible oscillation the total peak-to-peak swing across the tuned circuit and the Source should not exceed the supply voltage.

TEST RESULTS

The circuit was checked out on a bread-board at frequencies up to 400MHz and showed no noticeable odd harmonics and even harmonics down -50dB. In computer analysis the circuit was simulated without the feedback loop by inserting a signal into the Source connection as in the actual circuit.

The following computed data shows phase and amplitude response of the tuned circuit and the feedback port.

Figure 2. TZ403BD Oscillator Response

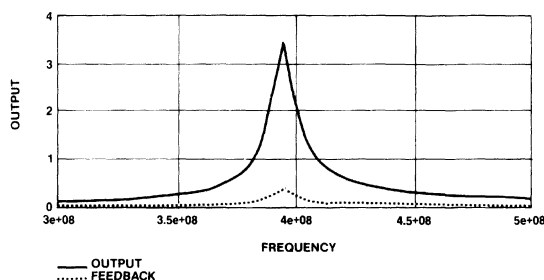
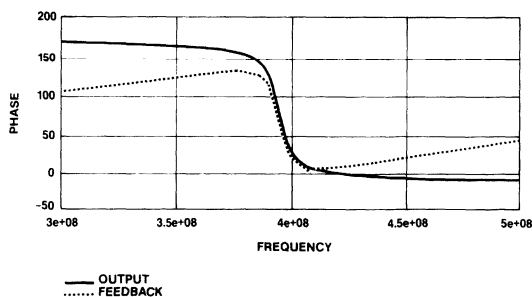


Figure 3. TZ403BD Oscillator Phase



CONCLUSION

A damping resistor may have to be added across the tuned circuit to maintain a constant "Q" with device and other component variations. The capacitor divider should be around 5:1 for a "Q" of 25. For higher "Q" values the ratio has to increase. Since the TZ403BD has very low interelectrode capacitances, the stability of the tuned circuit will be mostly determined by external components.

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